Preliminary Information

AMD

AMD-751™

System Controller

Data Sheet

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Revision History

Date	Rev	Description
August 1999	D	Initial public release

Conventions, Abbreviations, and References

This section contains information about the conventions and abbreviations used in this document and a list of related publications.

Signals and Bits

- Active-Low Signals—Signal names containing a pound sign, such as SFILL#, indicate active-Low signals. They are asserted in their Low-voltage state and negated in their High-voltage state. When used in this context, High and Low are written with an initial upper case letter.
- Signal Ranges—In a range of signals, the highest and lowest signal numbers are contained in brackets and separated by a colon (for example, D[63:0]).
- Reserved Bits and Signals—Signals or bus bits marked *reserved* must be driven inactive or left unconnected, as indicated in the signal descriptions. These bits and signals are reserved by AMD for future implementations. When software reads registers with reserved bits, the reserved bits must be masked. When software writes such registers, it must first read the register and change only the non-reserved bits before writing back to the register.
- Three-State—In timing diagrams, signal ranges that are high impedance are shown as a straight horizontal line half-way between the high and low levels.
- Invalid and Don't-Care—In timing diagrams, signal ranges that are invalid or don't-care are filled with a screen pattern.

Data Terminology

The following list defines data terminology:

- Quantities
  - A *word* is two bytes (16 bits)
  - A *doubleword* is four bytes (32 bits)
  - A *quadword* is eight bytes (64 bits)
  - An AMD Athlon™ processor cache line is eight quadwords (64 bytes)

- Addressing—Memory is addressed as a series of bytes on eight-byte (64-bit) boundaries in which each byte can be separately enabled.
- Abbreviations—The following notation is used for bits and bytes:
  - Kilo (K, as in 4-Kbyte page)
  - Mega (M, as in 4 Mbits/sec)
  - Giga (G, as in 4 Gbytes of memory space)

  See Table 2 for more abbreviations.
- Little-Endian Convention—The byte with the address xx...xx00 is in the least-significant byte position (little end). In byte diagrams, bit positions are numbered from right to left—the little end is on the right and the big end is on the left. Data structure diagrams in memory show low addresses at the bottom and high addresses at the top. When data items are aligned, bit notation on a 64-bit data bus maps directly to bit notation in 64-bit-wide memory. Because byte addresses increase from right to left, strings appear in reverse order when illustrated.
- Bit Ranges—In text, bit ranges are shown with a dash (for example, bits 9–1). When accompanied by a signal or bus name, the highest and lowest bit numbers are contained in brackets and separated by a colon (for example, AD[31:0]).
- Bit Values—Bits can either be set to 1 or cleared to 0.
- Hexadecimal and Binary Numbers—Unless the context makes interpretation clear, hexadecimal numbers are followed by an h and binary numbers are followed by a b.

Abbreviations and Acronyms

Table 2 contains the definitions of abbreviations used in this document.

Table 1. Abbreviations

Abbreviation	Meaning
A	Ampere
F	Farad
G	Giga-
Gbit	Gigabit
Gbyte	Gigabyte

Table 1. Abbreviations (Continued)

Abbreviation	Meaning
H	Henry
h	Hexadecimal
K	Kilo-
Kbyte	Kilobyte
M	Mega-
Mbit	Megabit
Mbyte	Megabyte
MHz	Megahertz
m	Milli-
ms	Millisecond
mW	Milliwatt
μ	Micro-
μA	Microampere
μF	Microfarad
μH	Microhenry
μs	Microsecond
μV	Microvolt
n	nano-
nA	nanoampere
nF	nanofarad
nH	nanohenry
ns	nanosecond
ohm	Ohm
p	pico-
pA	picoampere
pF	picofarad
pH	picohenry
ps	picosecond
s	Second
V	Volt
W	Watt

Table 2 contains the definitions of acronyms used in this document.

Table 2. Acronyms

Abbreviation	Meaning
AAT	AGP Address Translator
ACK	Acknowledge
ACPI	Advanced Configuration and Power Interface
AGP	Accelerated Graphics Port
APCI	AGP Peripheral Component Interconnect
API	Application Programming Interface
APIC	Advanced Programmable Interrupt Controller
ATE	Address Translation Engine
AWQ	PCI/APCI Write Queue
AXQ	AGP Transaction Queue
BAR	Base Address Register
BIOS	Basic Input/Output System
BIST	Built-In Self-Test
BIU	Bus Interface Unit
CS	Chip Select
CSQ	System Data and Control Queue
CQ	Command Queue
DDR	Double-Data Rate
DIMM	Dual Inline Memory Module
DMA	Direct Memory Access
DRAM	Direct Random Access Memory
ECC	Error Correcting Code
EIDE	Enhanced Integrated Device Electronics
EISA	Extended Industry Standard Architecture
EPROM	Enhanced Programmable Read Only Memory
EV6	Digital™ Alpha™ Bus
FID	Frequency Integer Divisor
FIFO	First In, First Out
GART	Graphics Address Remapping Table
GDC	GART Directory Cache
GFE	GART Front End
GTC	GART Table Cache

Table 2. Acronyms (Continued)

Abbreviation	Meaning
GTW	GART Table Walk
HSTL	High-Speed Transistor Logic
IACK	Interrupt Acknowledge
IDE	Integrated Device Electronics
IMB	Interrupt Message Bus
ISA	Industry Standard Architecture
JEDEC	Joint Electron Device Engineering Council
JTAG	Joint Test Action Group
LAN	Large Area Network
LRU	Least-Recently Used
LSB	Least Significant Bit
LVTTL	Low Voltage Transistor Transistor Logic
MA	Memory Address
MCT	Memory Controller
MD	Memory Data
MDA	Monochrome Display Adapter
MDP	Memory Data Path
MQA	Memory Queue Arbiter
MRA	Memory Request Arbiter
MRF	Memory Read FIFO
MRL	Memory Read Line
MRM	Memory Read Multiple
MRO	Memory Request Organizer
MRQ	Memory Read Queue
MRS	Memory Request Scheduler
MSB	Most Significant Bit
MTRR	Memory Type and Range Registers
MWF	Memory Write FIFO
MWI	Memory Write-and-Invalidate
MWQ	Memory Write Queue
MWS	Memory Write Selector
MUX	Multiplexer
NMI	Non-Maskable Interrupt
OD	Open Drain

Table 2. Acronyms (Continued)

Abbreviation	Meaning
PBGA	Plastic Ball Grid Array
PA	Physical Address
PCI	Peripheral Component Interconnect
PDE	Page Directory Entry
PDT	Page Directory Table
PH	Page Hit
PLL	Phase Locked Loop
PMSM	Power Management State Machine
POS	Power-On Suspend
POST	Power-On Self-Test
PPA	Physical Page Address
PPQ	Pending Probes Queue
PQ	Probe Queue
PRA	Probe Response Alert Agent
PSQ	Probe System Data and Control Queue
PT	Page Tables
PTE	Page Table Entries
RAM	Random Access Memory
RBN	Round Robin
RDQ	Read Request Queue
ROM	Read Only Memory
RXA	Read Acknowledge Queue
SBA	Sideband Address
SDI	System DRAM Interface
SDRAM	Synchronous Direct Random Access Memory
SIP	Serial Initialization Packet
SMbus	System Management Bus
SMC	SDRAM Memory Controller
SPD	Serial Presence Detect
SRAM	Synchronous Random Access Memory
SROM	Serial Read Only Memory
SRQ	SysDC Read Queue
SysDC	System Data Commands
TLB	Translation Lookaside Buffer
TOM	Top of Memory
TTL	Transistor Transistor Logic

Table 2. Acronyms (Continued)

Abbreviation	Meaning
VAS	Virtual Address Space
VPA	Virtual Page Address
VGA	Video Graphics Adapter
WHAMI	Who Am I
WBT	Write Buffer Tag
WP	Write Protect
WRQ	Write Request Queue
USB	Universal Serial Bus
XCA	Transaction Combiner Agent
ZDB	Zero Delay Buffer

Related Publications

The following books discuss various aspects of computer architecture that may enhance your understanding of AMD products:

AMD Publications

AMD Athlon™ Processor Data Sheet, order# 21016

AMD-756™ Peripheral Bus Controller Data Sheet, order# 22548

Bus Architecture

PCI Local Bus Specification, Revision 2.2, PCI Special Interest Group, Hillsboro, Oregon, 1998.

AT Bus Design, Edward Solari, IEEE P996 Compatible, Annabooks, San Diego, CA, 1990.

Accelerated Graphics Port Interface Specification Revision 2.0, Intel Corporation, AGP Forum, 1998.

x86 Architecture

Programming the 80386, John Crawford and Patrick Gelsinger, Sybex, San Francisco, 1987.

80x86 Architecture & Programming, Rakesh Agarwal, Volumes I and II, Prentice-Hall, Englewood Cliffs, NJ, 1991.

General References

Computer Architecture, John L. Hennessy and David A. Patterson, Morgan Kaufman Publishers, San Mateo, CA, 1990.

Websites

Visit the AMD website for documentation of AMD products.

www.amd.com

Other websites of interest include the following:

- JEDEC home page—www.jedec.org
- IEEE home page—www.computer.org
- AGP Forum—www.agpforum.org

1 Features

The AMD Athlon™ processor powers the next generation in computing platforms, delivering the ultimate performance for cutting-edge applications and an unprecedented computing experience.

The AMD-750™ chipset is a highly integrated system logic solution that delivers enhanced performance for the AMD Athlon processor and other AMD Athlon system bus-compatible processors. The AMD-750 chipset consists of the AMD-751™ system controller in a 492-pin plastic ball-grid array (PBGA) package and the AMD-756™ peripheral bus controller. The AMD-751 system controller features the AMD Athlon system bus, system memory controller, accelerated graphics port (AGP) controller, and peripheral component interconnect (PCI) bus controller. Figure 1 on page 6 shows a block diagram for the AMD-750 chipset.

The AMD-751 system controller is designed with the following features:

- The AMD Athlon system bus supports three 200-MHz high-speed channels
- The 33-MHz 32-bit PCI 2.2-compliant bus interface supports up to six masters
- The 66-MHz AGP 2.0-compliant interface supports 2x data transfer mode
- High-speed memory—The AMD-751 system controller is designed to support a 100-MHz PC-100 Rev. 1.0 SDRAM DIMMs

This document describes the features and operation of the AMD-751 system controller. For a description of the AMD-756 peripheral bus controller, see the *AMD-756™ Peripheral Bus Controller Data Sheet*, order# 21645. Key features of the AMD-751 system controller are provided in this section.

1.1 AMD Athlon™ System Bus

The AMD Athlon system bus has the following features:

- High-performance point-to-point system bus topology
- Source-synchronous clocking for high-speed transfers
- HSTL-like low-voltage swing transceiver logic signal levels
- Three 200-MHz independent high-speed channels:
  - 13-pin processor request channel
  - 13-pin system probe channel
  - 72-pint data transfer channel (8-bit ECC)
- 1.6 Gigabyte per second peak data transfer rates at 200 MHz
- Large 64-byte (cache line) data burst transfers
- Data Buffers:
  - Memory write FIFO (MWF)
  - Memory read FIFO (MRF)
  - PCI/APCI (AGP-PCI) write buffer
  - PCI/APCI read buffer
- Transaction Queues:
  - Command queue (CQ)
  - Memory write queue (MWQ)
  - Memory read queue (MRQ)
  - Probe (snoop) queue (PQ)

1.2 Integrated Memory Controller

The integrated memory controller has the following features:

- Memory Request Organizer (MRO)—Serves as a data crossbar, determines request dependencies, and optimizes scheduling of memory requests
- The AMD-751 system controller supports the following concurrences:
  - Processor-to-main-memory with PCI-to-main-memory
  - Processor-to-main-memory with AGP-to-main-memory
  - Processor-to-PCI with PCI-to-main-memory or AGP-to-main-memory

- Memory error correcting code (ECC) support
- Supports the following DRAM:
  - Up to three non-buffered PC-100 Rev. 1.0 SDRAM DIMMs using 16-Mbit, 64-Mbit, and 128-Mbit technology (See Table 3 on page 9)
  - 64-bit data width, plus 8-bit ECC paths
  - Flexible row and column addressing
- Supports up to 768 Mbytes of memory
- Four open pages within one CS (device selected by chip select) for one quadword
- Default two-page leapfrog policy for eight quadword requests
- BIOS-configurable memory-timing parameters and configuration parameters
- 3.3-V memory interface operation with no external buffers
- Four cache lines of processor-to-DRAM posted write buffers with full read-around capability
- Concurrent DRAM writeback and read-around-write
- Burst read and write transactions
- Decoupled and burst DRAM refresh with staggered CS timing
- Provides the following refresh options:
  - Programmable refresh rate
  - CAS-before-RAS
  - Populated banks only
  - Chipset powerdown via SDRAM automatic refresh command
  - Automatic refresh of idle slots—improves bus availability for memory access by the processor or system

1.3 PCI Bus Controller

The PCI bus controller has the following features:

- Compliance with *PCI Local Bus Specification, Revision 2.2*
- Supports six PCI masters
- 32-bit interface, compatible with 3.3-V and 5-V PCI I/O
- Synchronous PCI bus operation up to 33 MHz
- PCI-initiator peer concurrence
- Automatic processor-to-PCI burst cycle detection
- Four-entry, 64-bit PCI master (processor or AGP) write FIFO
- Extensive utilization of FIFOs
- Zero wait-state PCI initiator and target burst transfers
- PCI-to-DRAM data streaming up to 132 Mbytes per second
- Enhanced PCI command optimization, such as memory read line (MRL), memory read multiple (MRM), and memory-write-and-invalidate (MWI)
- Timer-enforced fair arbitration between PCI initiators
- Supports advanced concurrency
- Supports retry disconnect for improved bus utilization
- PCI read buffer keeps track of each master
- PCI target request queue

1.4 AGP Features

The AGP features include the following:

- Bus Features
  - Compliance with AGP 2.0 specification
  - Synchronous 66-MHz 1x and 2x data-transfer modes
  - Multiplexed and demultiplexed transfers
  - Up to four pipelined grants
  - Support of sideband address (SBA) bus
- Request Queue Features
  - Separate read-request and write-request queues
  - Reordering of high-priority requests over low-priority requests in queue

- Simultaneous issuing of requests from both the write queue and read queue
- Selects next request to optimize bus utilization

- Transaction Queues
  - Memory-to-AGP and processor-to-AGP transaction queues
- FIFO Features
  - 16-entry (64-bit) AGP-to-memory write FIFO
  - 64-entry (64-bit) memory-to-AGP read FIFO
- Secondary PCI Bus Features
  - Pipelined burst reads and writes
  - Extensive utilization of FIFOs
- GART (graphics address remapping table) Features
  - Conventional (two-level) GART scheme
  - Eight-entry, fully-associative GART table cache (GTC)
  - Three fully-associative GART directory caches (GDC)
    - One 4-entry for PCI
    - One 8-entry for the processor
    - One 16-entry for AGP

1.5 Power Management

The power management features include the following:

- Compliance support for both ACPI and Microsoft® PC 98 power management
- The AMD-751 system controller supports the following power states:
  - Processor Halt/Stop Grant/Sleep states
  - Power-On Suspend

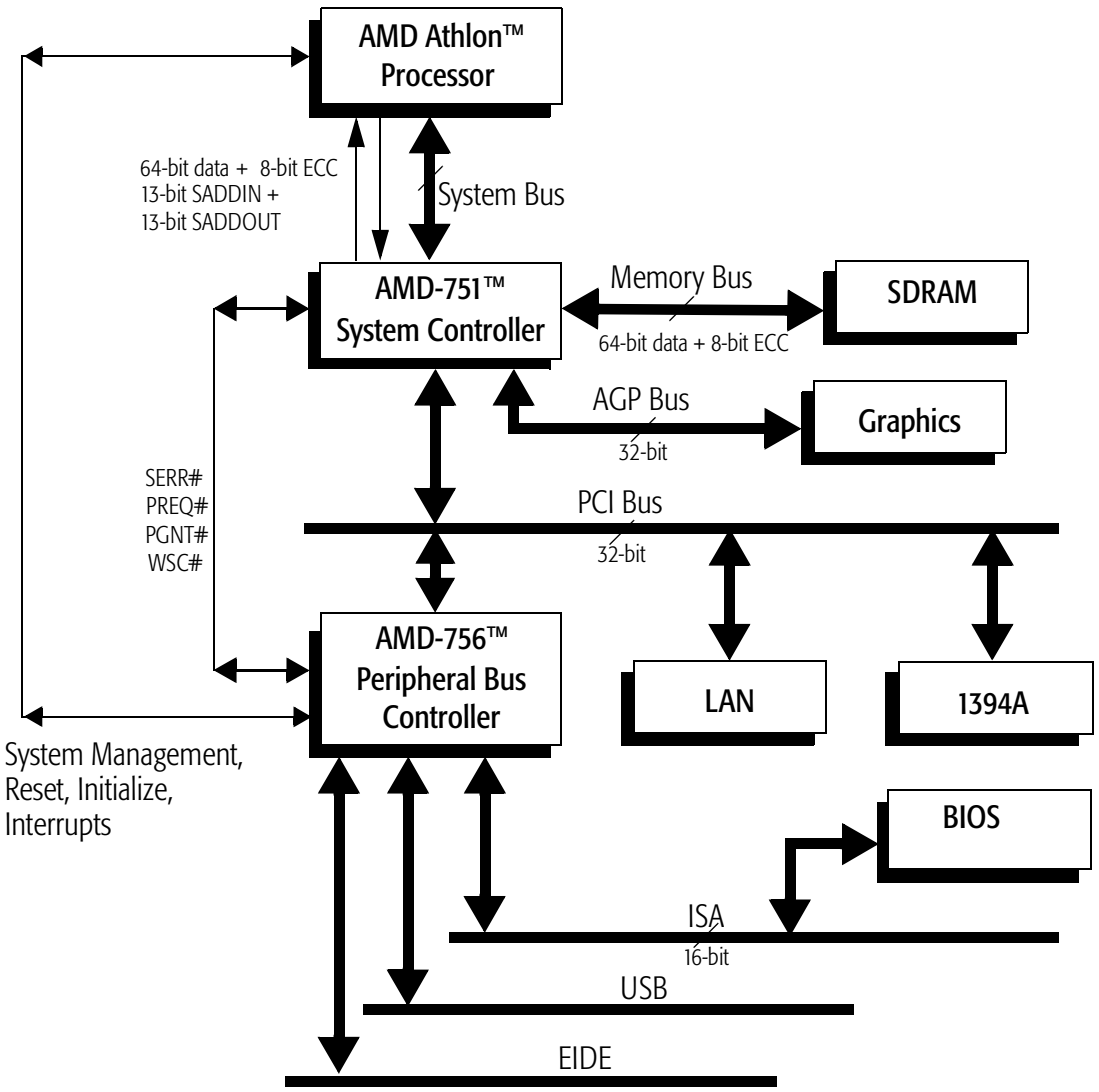


Figure 1. AMD-750™ Chipset System Block Diagram

2 Overview

The AMD-751 system controller is designed to optimize the interaction between the processor, DRAM, AGP, and the PCI bus with pipelined burst and concurrent transactions. Each bus interface includes multiple specialized FIFO buffers to enable optimum system concurrency. In the AMD-751, AMD has introduced a memory-request organizer to optimize the bandwidth of the DRAM. The AMD-751 system controller implements the AGP to provide streamlined 3D renderings and reduce graphics memory requirements. The AMD-751 is packaged in a 492-pin PBGA.

2.1 System

The AMD-751 system controller is capable of performing I/O transactions, single-access memory transactions, and block-access memory transactions. The AMD Athlon system bus is a split-transaction bus. A split-transaction bus optimizes system throughput by allowing the AMD-751 system controller to schedule tasks and thereby free the bus during resource delays.

The system controller responds only to I/O cycles within its configuration-register space and to memory requests as defined in its configuration registers.

All timing on the system bus is derived from the system clock (SYSCLK).

2.1.1 Processor Interface

The AMD Athlon system bus consists of three independent high-speed channels, including a 72-bit, 200-MHz, point-to-point, non-multiplexed, source-synchronous clocked data transfer channel capable of supporting the AMD Athlon processor with transfer rates of 1.6 Gigabyte per second. To achieve higher speed data transfers, the AMD Athlon system bus uses an open-drain, HSTL-like signaling level. Source-synchronous clocking compensates for PC board propagation delays to enable higher speed transfers.

The AMD-751 processor interface responds to processor commands, issues probes, and controls all data movement into and out of the processor. More details on the processor interface can be found in Chapter 5, "Functional Operation" starting on page 45.

2.1.2 Memory Controller

The AMD-751 system controller incorporates a high-performance DRAM controller with a memory-request organizer that provides the DRAM interface for an AMD Athlon processor and can support PC-100 Rev. 1.0 SDRAM DIMMs at 100 MHz. The memory-request organizer serves as a data crossbar and determines request dependencies to provide optimum scheduling of memory requests. Large on-chip FIFOs are used to decouple requests and provide concurrency. These features combine with the split-transaction processor bus to facilitate optimum use of the bus and memory bandwidths. The memory controller can address up to three slots of SDRAM at 100 MHz in various combinations, up to a total of 768 Mbytes.

The AMD-751 system controller supports the following concurrencies:

- Processor-to-main-memory with PCI-to-main-memory
- Processor-to-main-memory with AGP-to-main-memory
- Processor-to-PCI-memory with PCI-to-main-memory or AGP-to-main-memory

PC-100 Rev. 1.0 SDRAMs DIMMs allow fast bursting of data between the DRAM and the internal controller data buffers at 100 MHz. The DRAM controller supports a 72-bit data path to memory and can be configured to support error correcting code (ECC), which can correct single-bit errors and detect double-bit errors for data integrity. The BIOS must determine the type of memory installed and program the configuration registers accordingly.

The AMD-751 supports the SDRAM types shown in Table 3 on page 9. It does not support x32 DRAM configurations in the 16-Mbit technology. The AMD-751 logically supports the x4 configuration, but it is not recommended with unbuffered DIMMs.

Table 3. SDRAM Organizations Supported

SDRAM Organization	Banks	Addressing
16M x 4	2	10 x 11
16M x 8	2	9 x 11
16M x 16	2	8 x 11
16M x 32	Not Supported	
64M x 4	4	10 x 12
64M x 4	2	10 x 13
64M x 8	4	9 x 12
64M x 8	2	9 x 13
64M x 16	4	8 x 12
64M x 16	2	8 x 13
64M x 32	4	7 x 12
64M x 32	2	7 x 13
128M x 4	4	11 x 12
128M x 8	4	10 x 12
128M x 16	4	9 x 12
128M x 32	4	8 x 12

For more details on the memory controller, see Chapter 5, "Functional Operation" starting on page 45.

2.1.3 PCI Controller

The AMD-751 system controller is compatible with the *PCI Local Bus Specification, Revision 2.2*. It can operate at either 3.3 V or 5 V, and offers 64-bit to 32-bit data conversion. The AMD-751 supports up to six external PCI masters.

The AMD-751 implements a very high degree of internal concurrency. However, all PCI-to-memory transactions are, by definition, coherent and therefore must be snooped in all processors.

Five separate PCI FIFOs containing over 300 bytes of storage are utilized to facilitate concurrency. In addition, the AMD-751 prefetches eight quadwords (one AMD Athlon processor cache line) when performing memory reads for a PCI master.

Enhanced PCI bus commands, such as memory read line (MRL), memory read multiple (MRM), and memory

write-and-invalidate (MWI), maximize data throughput. The AMD-751 system controller employs a variety of techniques to minimize PCI initiator read latency and DRAM utilization. The combination of these features allows a PCI initiator to achieve the full 133-Mbyte burst transfer rate. In addition, the AMD-751 contains a PCI arbiter. See Chapter 5, "Functional Operation" starting on page 45 for more information.

2.1.4 Accelerated Graphics Port (AGP)

The accelerated graphics port (AGP) is an alternate interface bus for a computer system. The AGP provides a point-to-point link between a graphics controller and the memory controller. This additional pathway to memory removes 3D graphics traffic from the PCI bus and provides a special access path to main memory, allowing it to function as part of graphics memory and reducing the amount of memory required on the graphics adapter. Typically, the section of main memory allocated for the AGP adapter would then be used to hold 'textures', improving the realism of 3D images.

The AGP bus is essentially an expansion of the standard PCI local bus containing additional sideband signals and commands. The three primary enhancements to PCI include pipelined memory requests, separate address and data buses, and double-pumped (2x) AC timing mode, in which data is transferred on both edges of the AGP clock. Double-pumping enables effective transfer rates as high as 133 MHz, generating an effective data transfer rate of up to 533 Mbytes/second.

The AGP bus supports PCI as well as AGP transfers. As usual, the A_FRAME# signal indicates PCI transfers, while a new signal, PIPE#, is used to signify AGP transfers. To avoid confusion in this document, the system-wide PCI bus is referred to as the primary PCI bus, and the PCI implementation on the AGP bus is referred to as the secondary PCI bus or A-PCI.

The AMD-751 implements an AGP 1.0-compliant interface, which provides a 32-bit-wide data path operating at either 66 MHz or 133 MHz. The AMD-751 can queue 16 outstanding AGP transactions. See Chapter 5, "Functional Operation" starting on page 45 for more information.

The AMD-751 system controller functions as a PCI target on the AGP bus. When the AGP bus functions in AGP mode, the graphics controller is the AGP initiator and the AMD-751, which contains the memory controller, functions as the AGP target.

The AMD-751 implements a full-featured graphics-address remapping table (GART). As shown in Table 4, this GART implementation is distributed with individual table caches at each interface and a common directory cache in the table-walk logic that contains four fully associative entries. See Chapter 5, "Functional Operation" starting on page 45 for more details on the GART.

Table 4. GART Table-Cache Sizes

Interface	GART Table-Cache Size/Organization
AGP	16 Entries, fully associative
PCI & A-PCI	4 Entries, fully associative
Processor	8 Entries, fully associative

2.1.5 Block Diagram

Figure 2 shows the full complement of features and functions built into the AMD-751 system controller system logic.

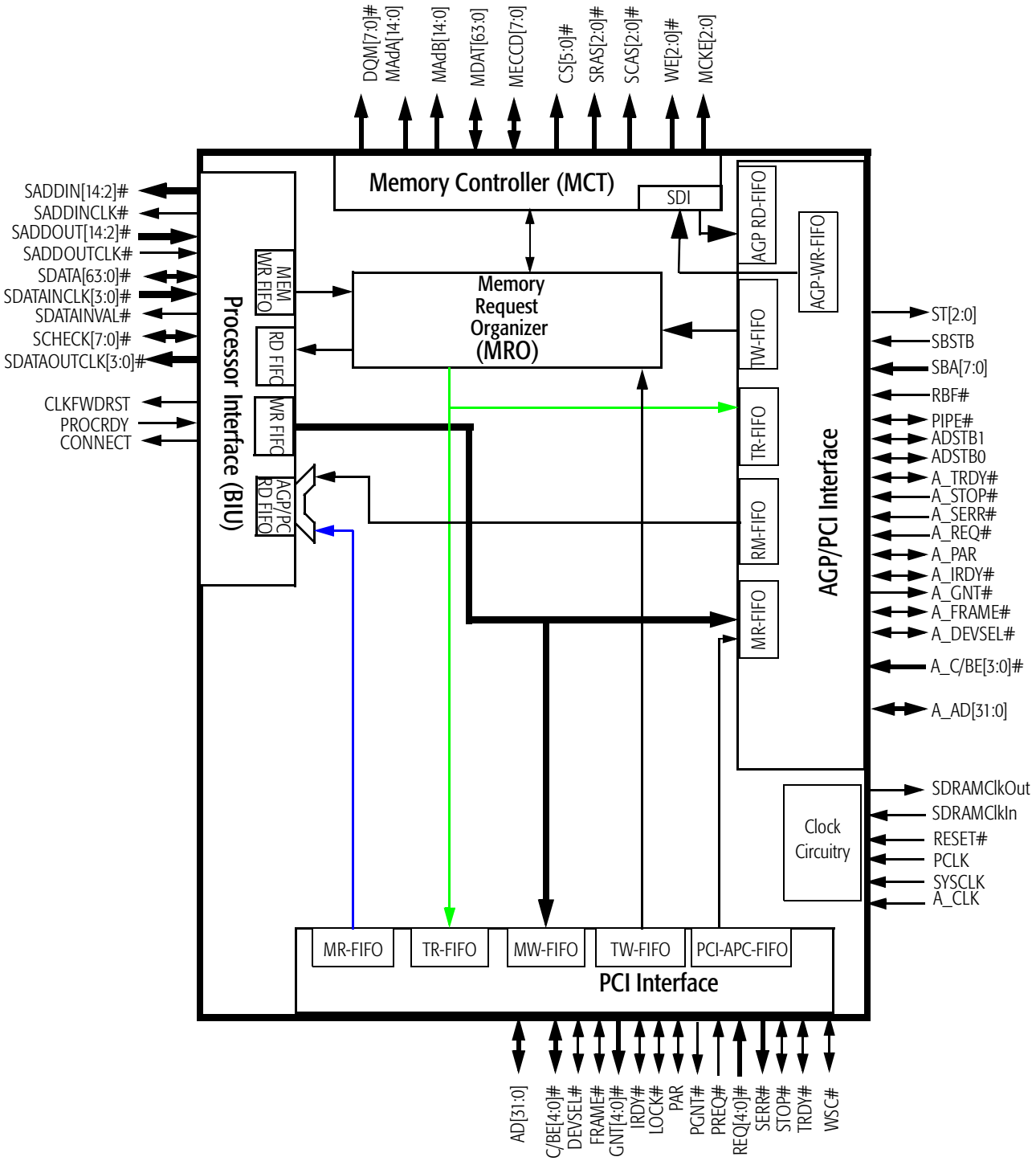


Figure 2. AMD-751™ System Controller Block Diagram

2.1.6 Package

The AMD-751 is packaged in a 492-ball, 35-mm plastic ball grid array (PBGA).

2.1.7 Power

The AMD-751 operates from a 3.3-V V_{dd} supply and dissipates 4.5 watts (W) operating under worst-case conditions. (Maximum V_{dd} is with heavy bus traffic.)

The AMD-751 implements the power-on-suspend (POS) power management state. To implement the POS state, the AMD-751 provides two facilities—SDRAM self-refresh and PCI master grant suspend.

SDRAMs are put in a self-refresh mode by the deassertion of the MCKE[2:0] pins. The AMD-751 enters that mode in a Stop Grant state. Careful routing of this signal on the board is important to ensure that it stays clean when it is asserted or deasserted. PCI master grants are disabled via register bit 0 in BAR2 offset 0h (see page 177).

2.2 Interface Levels

A complete pinout is shown in Chapter 12, "Package Specifications" on page 201. The rough grouping of signal types is shown in Table 5.

Table 5. AMD-751™ System Controller Interface Voltages

Interface	Group	Voltages
Processor	OD	Open drain, pulled to 1.6 V
SDRAM	LVTTL	3.3 V
PCI	PCI	3.3 V, 5 V tolerant
AGP	AGP	3.3 V

2.3 Clocking

The AMD-751 system controller receives a 100-MHz system clock and a 33-MHz PCI clock. The AMD-751 generates and drives the 100-MHz SDRAM clocks through a zero-delay buffer. The 66-MHz AGP clock is provided by the system clock generator as shown in Figure 3. It uses a non-JTAG, partial-scan scheme for silicon and motherboard testability (NAND tree).

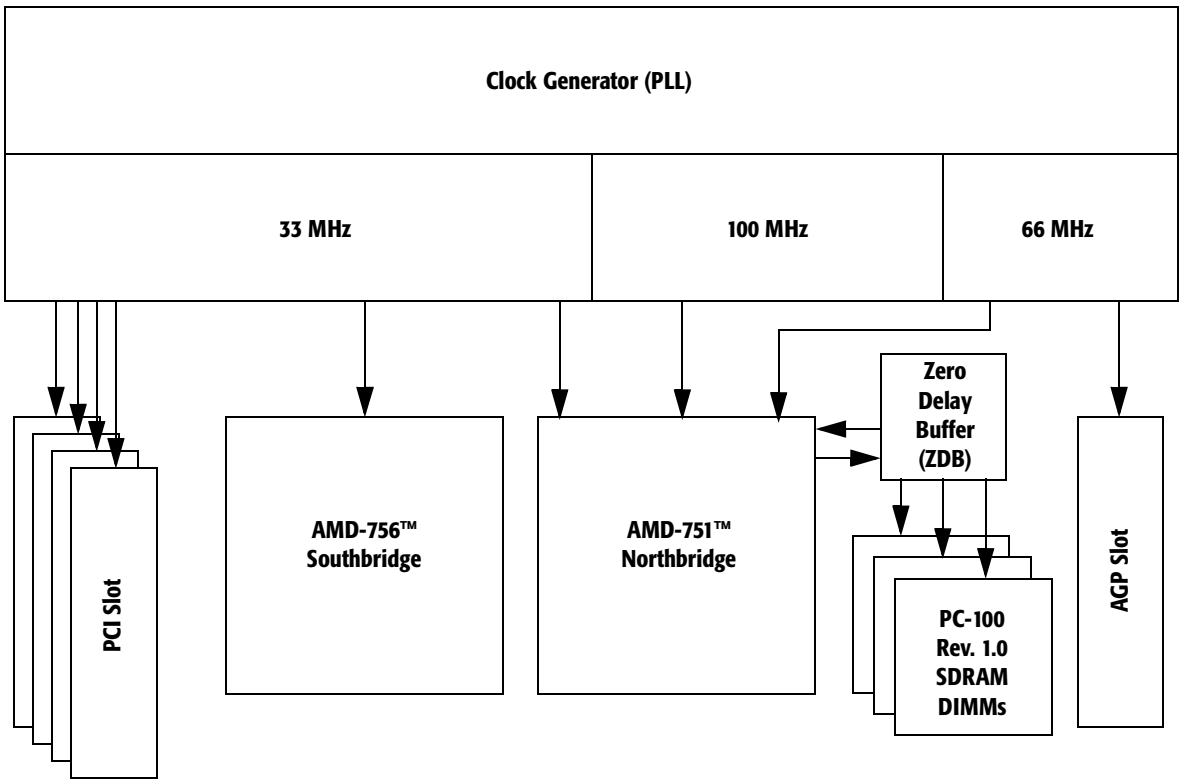


Figure 3. AMD Athlon™ Processor-Based System Clocking

3 Ordering Information

AMD standard products are available in several packages and operating ranges. The order number is formed by a combination of the elements shown in Figure 4. Table 6 shows valid combinations of elements. Contact your AMD representative for detailed ordering information.

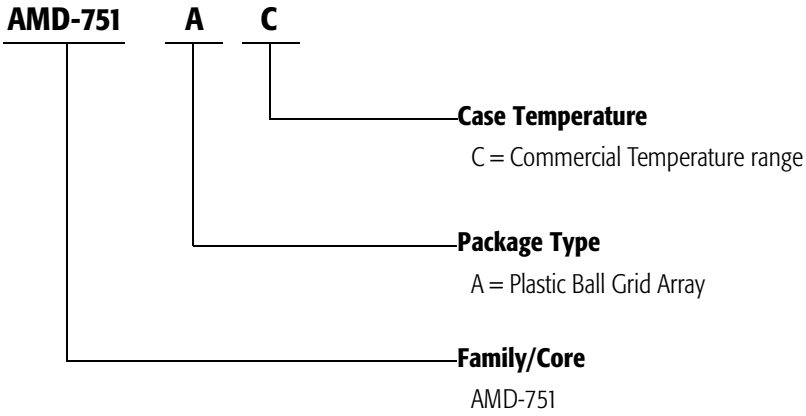


Figure 4. Ordering Information Elements

Table 6. Valid Combinations for Ordering Parts

OPN	Package Type	Operating Voltage	Case Temperature
AMD-751AC	492-pin PBGA ATX	3.135 V–3.6 V	85°C

Note:
Valid combinations are configurations that are or will be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

4 Signal Descriptions

4.1 Processor Interface Signals

4.1.1 CLKFWDRST (Clock Forward Reset)

Output

Summary CLKFWDRST resets the source-synchronous clock circuitry for the processor.

Driven This signal is negated by RESET#. It is asserted off the rising edge of SYSCLK.

4.1.2 CONNECT (Connect)

Output

Summary CONNECT is an output from the AMD-751 system controller and is used for power management and source-synchronous clock initialization at reset.

Driven This signal is negated by RESET#. It is asserted off the rising edge of SYSCLK.

4.1.3 PROCRDY (Processor Ready)

Input

Summary PROCRDY is an input to the AMD-751 system controller and is used for power management and source-synchronous clock initialization at reset.

Sampled This signal is sampled on the rising edge of SYSCLK.

4.1.4 SADDIN[14:2]# (Address/Command)

Output

Summary The SADDIN[14:2]# bus is the unidirectional system probe channel to the processor. It is used to transfer probes or data movement commands into the processor. All probes and commands on the SADDIN[14:2]# channel are skew-aligned with the source-synchronous clock, SADDINCLK#.

During PCI-to-DRAM cycles, the AMD-751 system controller drives the SADDIN[14:2]# bus to snoop (inquire cycle) the processor cache.

Driven The AMD-751 system controller drives the SADDIN[14:2]# channel on each edge of SADDINCLK#.

4.1.5 SADDINCLK# (System Address In Clock)

Output

Summary SADDINCLK# is the single-ended source-synchronous clock for the SADDIN[14:2]# bus driven by the AMD-751 system controller. Each clock edge is used to transfer probes or data movement commands to the processor.

Driven This signal is driven inactive (negated) when the CLKFWDRST signal is active (true). When CLKFWDRST is deasserted, SADDINCLK# runs continuously.

4.1.6 SADDOUT[14:2]# (System Address Out)

Input

Summary The SADDOUT[14:2]# channel is the unidirectional system address interface from the processor to the AMD-751 system controller. The SADDOUT[14:2]# channel is used to transfer processor requests to the system. All commands on this channel are skew-aligned with the source-synchronous clock, SADDOUTCLK#.

Sampled

The SADDOUT[14:2]# channel is sampled by the AMD-751 system controller on each edge of SADDOUTCLK#.

The AMD-751 system controller samples commands driven by the processor on the SADDOUT[14:2]# channel and forwards them to the PCI bus, AGP bus, or DRAM, depending on the address range and AMD-751 configuration.

4.1.7 SADDOUTCLK# (System Address Out Clock)

Input

Summary

SADDOUTCLK# is the single-ended source-synchronous clock for the SADDOUT[14:2]# channel driven by the processor. Each edge is used to transfer commands.

This signal is driven inactive (negated) when the CLKFWDRST signal is active (true). When CLKFWDRST is deasserted, SADDOUTCLK# runs continuously.

4.1.8 SCHECK[7:0]# (Data Bus Check Byte)

Bidirectional

Summary

SCHECK[7:0]# contains the ECC check bits for data transferred on the SDATA[63:0]# bus.

Driven, Sampled, and Floated

As Outputs: The AMD-751 system controller drives SCHECK[7:0]# with valid data.

As Inputs: During write cycles, the AMD-751 system controller samples SCHECK[7:0]#.

SCHECK[7:0]# is floated out of RESET#. It remains floated except when driven with write data by the processor, by read data (writeback data) from the cache, or by read data from the AMD-751 system controller.

4.1.9 SDATA[63:0]# (Processor Data Channel)

Bidirectional

Summary

The SDATA[63:0]# channel is the bidirectional interface to and from the processor and system for data movement. Data is skew-aligned with either SDATAINCLK[3:0]# or SDATAOUTCLK[3:0]#. Each edge is used to transfer data.

Note: *In/Out is relative to the processor.*

The SDATA[63:0]# channel connects to the 64-bit data channel of the processor. Each of the four words of data that comprise this channel is qualified by a corresponding clock (SDATAINCLK[3:0]# or SDATAOUTCLK[3:0]#).

Driven, Sampled, and Floated

As Outputs: The AMD-751 system controller drives the SDATA[63:0]# channel with valid data on each edge of the system address clocks (SDATAINCLK[3:0]#).

As Inputs: During write cycles, the AMD-751 system controller samples the SDATA[63:0]# channel on each edge of SDATAOUTCLK[3:0]#.

SDATA[63:0]# is floated out of RESET#. It remains floated except when driven with write data by the processor, by read data (writeback data) from the cache, or by read data from the AMD-751 system controller.

4.1.10 SDATAINCLK[3:0]# (System Data In Clock)

Output

Summary

SDATAINCLK[3:0]# is the single-ended source-synchronous clock driven by the AMD-751 system controller to transfer data on SDATA[63:0]#. Each 16-bit data word is skew-aligned with this clock. Each edge is used to transfer data.

Driven

This signal is driven inactive (negated) when the CLKFWDRST signal is active (true). When CLKFWDRST is deasserted, SDATAINCLK# runs continuously.

4.1.11 SDATAINVAL# (System Data In Valid)

Output

Summary SDATAINVAL# is driven by the AMD-751 system controller and controls the flow of data into the processor. SDATAINVAL# can be used to introduce an arbitrary number of cycles between octawords (128 bits).

Driven This signal is negated by RESET#. SDATAINVAL# is asserted off the rising edge of SADDINCLK.

4.1.12 SDATAOUTCLK[3:0]# (System Address Out Clock)

Input

Summary SDATAOUTCLK[3:0]# is the single-ended source-synchronous clock driven by the processor and is used to transfer data on the SDATA[63:0]# channel. Each 16-bit data word is skew-aligned with this clock. Each edge is used to transfer data.

This signal is driven inactive (negated) when the CLKFWDRST signal is active (true). When CLKFWDRST is deasserted, SDATAOUTCLK# runs continuously.

4.1.13 SYSCLK (System Clock)

Input

Summary SYSCLK is a single-ended input clock signal provided to the phase locked loop (PLL) of the AMD-751 system controller from the system-clock generator. It is set at 100 MHz operation.

4.2 PCI Interface Signals

4.2.1 AD[31:0] (PCI Address/Data Bus)

Bidirectional

Summary

The AD[31:0] bus contains the standard, multiplexed PCI address and data lines. AD[31:0] contains a physical address during the first clock of a PCI transaction, and data during subsequent clocks. The address is driven when FRAME# is asserted, and data is driven or received in subsequent cycles.

When the AMD-751 system controller is the PCI initiator, these lines are outputs during the address and write data phases of a transaction, and inputs during the read data phases.

When the AMD-751 is the PCI target, these lines are inputs during the address and write data phases of a transaction, and outputs during the read data phases.

Driven, Sampled, and Floated

As Outputs: As an initiator, the AMD-751 system controller drives AD[31:0] with a valid address off the first rising edge of PCLK after it becomes the PCI bus master. During the first clock that FRAME# is asserted, AD[31:0] contains the address. During subsequent clocks, AD[31:0] contains data.

As Inputs: The AMD-751 system controller samples AD[31:0] on the rising edge of PCLK. During the first clock after FRAME# is asserted, the AMD-751 loads the bus contents into its internal address register. On each subsequent clock in which both TRDY# and IRDY# are asserted, AD[31:0] loads data into its data FIFO.

AD[31:0] is floated for one clock in between the address phase and the data phase of a read transfer. AD[31:0] is also floated during RESET# and when there is no initiator driving the bus.

4.2.2 C/BE[3:0]# (PCI Command/Byte Enables)

Bidirectional

Summary

C/BE[3:0]# contain the PCI command during the first clock cycle that FRAME# is asserted. These signals serve as a byte-enable signal for subsequent cycles.

Driven, Sampled, and Floated

As Outputs: The AMD-751 system controller drives C/BE[3:0]# with a valid command or byte enables off the rising edge of PCLK.

As Inputs: When the AMD-751 system controller is a target, it samples C/BE[3:0]# on the rising edge of every PCLK. C/BE[3:0]# are qualified by FRAME# for commands and qualified by IRDY# and TRDY# for data.

C/BE[3:0]# are floated during RESET# and when there is no initiator driving the bus.

4.2.3 DEVSEL# (PCI Device Select)

Bidirectional

Summary

The AMD-751 system controller samples DEVSEL# when it is the initiator in a PCI cycle to determine if the target device has responded. The AMD-751 drives DEVSEL# when it is the targeted device in a PCI cycle.

Driven, Sampled, and Floated

As an Output: The AMD-751 system controller drives this signal when it decodes the address and determines it is the target of the transfer.

As an Input: When the AMD-751 system controller is the initiator, it samples this signal on the rising edge of every PCLK to determine that the target is present. The target must respond within eight clocks after FRAME# is asserted.

DEVSEL# is floated during RESET# and when there is no initiator driving the bus.

4.2.4 FRAME# (PCI Cycle Frame)

Bidirectional

Summary

The AMD-751 system controller asserts FRAME# at the beginning of a PCI cycle when it is the initiator, and holds it asserted until the beginning of the last data transfer in the cycle.

If the AMD-751 is the targeted PCI device, it samples and latches the C/BE[3:0]# and AD[31:0] signals and asserts DEVSEL# at the first PCLK edge on which it samples FRAME# asserted.

Driven, Sampled, and Floated

As an Output: The AMD-751 system controller drives FRAME# valid off the rising edge of PCLK. The duration of FRAME# varies with the length of the transfer.

As an Input: When the AMD-751 system controller is a target, it samples this signal on the rising edge of every PCLK. The assertion of FRAME# indicates the start of a cycle. FRAME# remains asserted during burst transfers.

FRAME# is floated during RESET# and when there is no initiator driving the bus.

4.2.5 GNT[4:0]# (PCI Bus Grant)

Output

Summary

As the PCI bus arbiter, the AMD-751 system controller asserts one of these device-specific bus grant signals off the rising clock edge to indicate to an initiator that it has been granted control of the PCI bus.

Driven

GNT[4:0]# signals are never floated. They are negated off the rising edge of the clock, indicating that no device has been granted the bus. One of the GNT[4:0]# signals is asserted off the rising edge of the clock, indicating the particular channel that is granted use of the bus.

4.2.6 IRDY# (Initiator Ready)

Bidirectional

Summary

IRDY# indicates that a PCI initiator is ready to complete the current data phase of the transaction. During a read cycle, IRDY# asserted indicates the master is ready to accept the data. During a write cycle, IRDY# asserted indicates that write data is valid on AD[31:0]. Data is transferred on the PCI bus on each PCLK in which both IRDY# and TRDY# are asserted. Wait states are inserted on the bus until both IRDY# and TRDY# are asserted together.

Driven, Sampled, and Floated

As an Output: When the AMD-751 system controller is the PCI initiator, it drives IRDY# asserted one PCLK after it asserts FRAME# and holds it asserted until one cycle before the end of all transactions. The AMD-751 does not terminate a read or write cycle until it samples both IRDY# and TRDY# asserted.

As an Input: IRDY# is sampled on every rising edge of PCLK, when the AMD-751 system controller is a PCI target. When IRDY# and TRDY# are both asserted, the controller advances the FIFO to the next data. If either signal is negated, the current data is held on the bus.

IRDY# is floated when there is no bus master currently driving the bus.

4.2.7 LOCK# (PCI Bus Lock)

Bidirectional

Summary

A PCI initiator asserts LOCK# to prevent other devices from accessing a targeted device during atomic transactions. Using LOCK# is not recommended because it is not supported by the AMD-751 system controller, and the system can hang if the initiator does not unlock the resource.

Driven, Sampled, and Floated

An 8.2-Kohm pullup resistor is required to keep LOCK# inactive, if it is not implemented on an initiator.

4.2.8 PAR (PCI Bus Parity)

Bidirectional

Summary PAR indicates even parity. The AMD-751 system controller drives PAR as a PCI initiator one clock after the address phase and each data write phase to generate even parity across A_AD[31:0] and A_C/BE[3:0]#. The AMD-751 drives PAR as a PCI target one clock after each data read phase. The AMD-751 does not support parity checking.

Driven, Sampled, and Floated *As an Output:* This signal is asserted off the rising edge of every PCLK.

As an Input: The AMD-751 system controller does not support parity checking.

PAR is only floated when changing bus ownership from one initiator to another.

4.2.9 PCLK (PCI Clock)

Input

Summary PCLK is a 33-MHz clock provided by the system clock generator. It is used by the AMD-751 logic in the PCI clock domain. PCLK to A_CLK (AGP clock) skew is +/– 500ps maximum.

4.2.10 PGNT# (PCI Grant to Peripheral Bus Controller)

Output

Summary PGNT# grants control of the PCI bus to the PCI-ISA/IDE bridge functions implemented in the AMD-756 peripheral bus controller.

Driven PGNT# is driven off the rising edge of PCLK. RESET# forces PGNT# inactive. PGNT# is asserted in response to a PREQ#.

4.2.11 PREQ# (PCI Request from Peripheral Bus Controller)

Input

Summary The AMD-751 system controller samples PREQ# to determine if the AMD-756 peripheral bus controller needs PCI bus access.

Sampled This signal is sampled by the rising edge of every PCLK. If asserted, the arbiter issues a PGNT# when the bus is available.

4.2.12 REQ[4:0]# (PCI Bus Request)

Input

Summary As the PCI bus arbiter, the AMD-751 system controller samples these device-specific bus request signals to determine if another agent requires control of the PCI bus.

Sampled These signals are sampled by the rising edge of every PCLK. If active, the arbiter issues the corresponding GNT[4:0]# when the bus is available.

4.2.13 RESET# (Reset)

Input

Summary Asserting RESET# resets the AMD-751 system controller and sets all register bits to their default values. Bidirectional signals are three-stated and outputs are driven inactive. This signal is driven by the PCIRST# signal from the AMD-756 peripheral bus controller.

Sampled This signal may be asynchronous to SYSCLK and PCLK. It is synchronized internally, therefore it must be active for a minimum of four PCLK periods.

4.2.14 SERR# (System Error)

Output

Summary The AMD-751 system controller, as a PCI agent, asserts SERR# off the rising edge of PCLK one clock after it detects a system error. SERR# is an input to the AMD-756 peripheral bus controller, which can be programmed to generate a non-maskable interrupt (NMI).

Driven and Floated SERR# is driven asserted on the rising edge of PCLK to indicate that a fatal condition has been detected by the AMD-751 system controller. This is an open-drain output—normally a pullup resistor keeps this signal negated.

4.2.15 STOP# (PCI Bus Stop)

Bidirectional

Summary As a PCI initiator, the AMD-751 system controller samples STOP# to determine if the target device requires it to abort or retry a transaction.

Sampled STOP# is sampled by the current initiator on the rising edge of every PCLK to determine if the current transaction should continue or be stopped.

4.2.16 TRDY# (Target Ready)

Bidirectional

Summary As a PCI initiator, the AMD-751 system controller samples TRDY# to determine when the target agent is able to complete the data phase of a transaction.

As a PCI target, the AMD-751 asserts TRDY# to indicate that it has latched the data on AD[31:0] during a write phase or driven the data on AD[31:0] during a read phase.

Driven, Sampled, and Floated *As an Output:* When the AMD-751 system controller is the PCI target, it asserts TRDY# when valid data is available on the bus (initiator read) or when there is room in its internal FIFO

(initiator write). The AMD-751 does not terminate a read or write cycle until it samples both IRDY# and TRDY# asserted.

As an Input: TRDY# is sampled on every rising edge of PCLK when the AMD-751 system controller is a PCI initiator. When IRDY# and TRDY# are both asserted, the controller advances the FIFO to the next data. If either signal is negated, the current data is held on the bus.

TRDY# is floated when there is no bus master currently driving the bus.

4.2.17 WSC# (Write Snoop Complete)

Bidirectional

Summary WSC# is asserted to indicate that all of the snoop activity on the processor bus on behalf of the last PCI-to-DRAM write transaction is complete and that an APIC interrupt message can be sent. This signal is used only in configurations where an I/O APIC is installed.

Driven and Floated WSC# is driven asserted on the rising edge of PCLK to indicate to the AMD-756 peripheral bus controller that all probes due to PCI DMA (direct memory access) are complete.

The AMD-756 peripheral bus controller requests that the AMD-751 system controller issue a Fence command to its buffers by placing a single PCLK pulse on WSC#. The AMD-751 then marks the data currently in its buffers and waits for this data to reach processor-accessible (coherent) space. When this data reaches processor-accessible space, the AMD-751 responds by sending a two-clock pulse back to the AMD-756 peripheral bus controller. After this pulse is received, the AMD-756 peripheral bus controller transmits the interrupt message over the interrupt message bus (IMB).

4.3 DRAM Interface Signals

4.3.1 CS[5:0]# (Chip Selects)

Output

Summary CS[5:0]# function as chip select signals for SDRAMs.

Driven These signals are negated by RESET#. The memory controller asserts or negates these signals off the rising edge of SYSCLK at the appropriate time in the memory access sequence. See Chapter 5, "Functional Operation" starting on page 45 for more information.

4.3.2 DQM[7:0]# (Data Mask)

Output

Summary DQM[7:0]# provides data masks for each byte during SDRAM write cycles.

Driven These control signals are negated by RESET#. The memory controller asserts or negates these signals off the rising edge of SYSCLK at the appropriate time in the memory access sequence. See Chapter 5, "Functional Operation" starting on page 45 for more information.

4.3.3 MAdA[14:0] and MAdB[14:0] (Memory Address)

Output

Summary The multiplexed row and column address bits MAdA[14:0] and MAdB[14:0] connect to the system SDRAMs. They can address any size DRAM from 4 Mbits to 128 Mbits (for example, 16 Mbits x 4 = 64 Mbits, 16 Mbits x 8 = 128 Mbits). Two identical sets of memory addresses are provided to reduce signal loading for motherboard designs with three DIMM slots.

Driven The memory controller asserts or deasserts these signals off the rising edge of SYSCLK at the appropriate time in the memory access sequence. See Chapter 5, "Functional Operation" starting on page 45 for more information.

4.3.4 MCKE[2:0] (SDRAM Clock Enable)

Output

Summary MCKE[2:0] are clock enable signals for the synchronous DRAM. They operate in parallel to drive greater loads than a single signal can support and are used for power saving modes.

Driven These control signals are driven inactive (negated) by RESET#. See Chapter 5, "Functional Operation" starting on page 45 for more information.

4.3.5 MDAT[63:0] (Memory Data)

Bidirectional

Summary MDAT[63:0] connect to the DRAM data I/O. They are driven by the DRAM during reads and are driven by the AMD-751 system controller during writes.

Driven, Sampled, and Floated *As Outputs:* These signals are driven with the data to be written on the rising edge of SDRAM_CLKOUT. The data changes at different times based on the type of memory and timing selected. See Chapter 5, "Functional Operation" starting on page 45 for more information.

As Inputs: MDAT[63:0] are sampled on the rising edge of SDRAM_CLKIN.

MDAT[63:0] are floated when neither the AMD-751 system controller or the memory are driving the bus.

4.3.6 MECCD[7:0] (Memory ECC)

Bidirectional

Summary MECCD[7:0] carry error correction codes for the eight bytes of data on MDAT[63:0]. These signals are inputs to the AMD-751 system controller during DRAM read cycles and outputs during DRAM write cycles.

Driven, Sampled, and Floated *As Outputs:* These signals are driven with the parity or ECC data on the rising edge of SYSCLK. They change at different times based on the type of memory and timing selected. See Chapter 5, "Functional Operation" starting on page 45 for more information.

As Inputs: MECCD[7:0] are sampled on the same rising edge of SYSCLK that samples MDAT[63:0].

MECCD[7:0] are floated when neither the AMD-751 system controller or the memory are driving the bus.

4.3.7 SCAS[2:0]# (SDRAM Column Address Strobes)

Output

Summary SCAS0#, SCAS1#, and SCAS2# are column address strobe signals for the synchronous DRAM. They operate in parallel to drive greater loads than a single signal can support.

Driven These control signals are driven inactive (negated) by RESET#. The memory controller asserts or negates these signals off the rising edge of SYSCLK at the appropriate time in the memory access sequence. See Chapter 5, "Functional Operation" starting on page 45 for more information.

4.3.8 SDRAM Clk_In

Input

Summary The SDRAM Clk_In signal is used to clock in the data returned from a SDRAM read operation. Data is clocked in on the rising edge of this signal. This clock is provided by the ZDB and is phase aligned with the SDRAM clocks.

4.3.9 SDRAM Clk_Out

Output

Summary SDRAM Clk_Out is a clock signal for the synchronous DRAM.

Driven This signal is a free-running clock generated by the internal PLL in the AMD-751 system controller. This signal is used to clock a zero delay buffer (ZDB) external to the AMD-751. The ZDB, in turn, generates the clock for the SDRAMs. The advantage of the ZDB is that the timing of the clocks to the SDRAM DIMMs can be adjusted.

4.3.10 SRAS[2:0]# (SDRAM Row Address Strobes)

Output

Summary SRAS0#, SRAS1#, and SRAS2# are row address strobe signals for the synchronous DRAM. They operate in parallel to drive greater loads than a single signal can support.

Driven These control signals are driven inactive (negated) by RESET#. The memory controller asserts or negates these signals off the rising edge of SYSCLK at the appropriate time in the memory access sequence. See Chapter 5, “Functional Operation” starting on page 45 for more information.

4.3.11 WE[2:0]# (SDRAM Memory Write Enables)

Output

Summary WE[2:0]# are write enable signals for all DRAM. They operate in parallel to drive greater loads than a single signal can support.

Driven These control signals are driven inactive (negated) by RESET#. The memory controller asserts or negates these signals off the rising edge of SYSCLK at the appropriate time in the memory access sequence. See Chapter 5, “Functional Operation” starting on page 45 for more information.

4.4 AGP/PCI Signals

The following signal descriptions apply to AGP bus signals when used for AGP transactions. The AGP bus can also perform PCI transactions, in which case the AGP bus pins function identically to their PCI bus pin equivalents (same pin names without the A_ prefix), as described in "PCI Interface Signals" on page 22.

4.4.1 A_AD[31:0] (Address/Data Bus)

Bidirectional

Summary

In multiplexed mode, the A_AD[31:0] bus contains an AGP address when PIPE# is sampled asserted and data when PIPE# is sampled negated.

In demultiplexed mode, the A_AD[31:0] bus contains only AGP data, while AGP addresses are provided on the sideband address signals SBA[7:0].

Driven, Sampled, and Floated

As Outputs: In demultiplexed mode, the AMD-751 system controller drives A_AD[31:0] with ADSTB[1:0] during data transfers to the graphics controller from the system controller. In multiplexed mode, the AMD-751 drives A_AD[31:0] with a valid address or data off the rising edge of SYSCLK during the return of read requests. In addition, A_AD[31:0] are driven during processor writes to the graphics controller.

As Inputs: In demultiplexed mode, the AMD-751 system controller samples A_AD[31:0] on the rising edge of every ADSTB[1:0] during data transfers from the graphics controller to the system controller. In multiplexed mode, A_TRDY# and A_IRDY# qualify the SYSCLK edges on which data is sampled.

A_AD[31:0] are floated for one clock between the address phase and the data phase of a read transfer. In addition, A_AD[31:0] are floated during reset and when the bus is idle.

4.4.2 A_C/BE[3:0]# (PCI Command/Byte Enables)

Bidirectional

Summary

In multiplexed mode, A_C/BE[3:0]# contain command information when PIPE# is sampled asserted (see page 40), and byte-enable signals when PIPE# is sampled negated.

For PCI cycles on the AGP bus, C/BE#[3:0] carry PCI commands during the first clock cycle that A_FRAME# is asserted. After the first clock, A_C/BE[3:0]# are byte enables.

In demultiplexed mode, the commands are sent on SBA[7:0], and A_C/BE[3:0]# function only as byte enable signals during data transactions. All four A_C/BE# signals are asserted in each AGP data transaction because the minimum AGP data size is four doublewords.

Driven, Sampled, and Floated

As Outputs: The AMD-751 system controller drives A_C/BE[3:0]# with valid command information off the rising edge of SYSCLK when A_FRAME# or PIPE# is asserted. The AMD-751 drives A_C/BE[3:0]# with valid byte enables off the rising edge of SYSCLK when A_FRAME# or PIPE# is negated.

As Inputs: When the AMD-751 system controller is a target, it samples A_C/BE[3:0]# on the rising edge of SYSCLK.

A_C/BE[3:0]# are floated during reset and when the bus is idle.

4.4.3 A_CLK (AGP Clock)

Input

Summary

A_CLK receives a 66-MHz clock from the system clock generator. A_CLK is used by the AMD-751 system controller logic in the AGP clock domain.

4.4.4 A_DEVSEL# (PCI Device Select)

Bidirectional

Summary A_DEVSEL# is used for PCI transfers on the secondary PCI bus. Its function is the same as that of DEVSEL# on the primary PCI bus (see page 23).

A_DEVSEL# is not used during AGP transfers.

4.4.5 A_FRAME# (PCI Cycle Frame)

Bidirectional

Summary A_FRAME# is used for PCI transfers on the secondary PCI bus. Its function is the same as that of FRAME# on the primary PCI bus (see page 24).

A_FRAME# is not used during AGP transfers.

4.4.6 A_GNT# (AGP Bus Grant)

Output

Summary As the AGP bus arbiter, the AMD-751 system controller asserts A_GNT# in response to A_REQ# from the initiator (graphics controller) to indicate to the initiator that it has been granted control of the bus. At the same time, the system controller provides status information on status signals ST[2:0] to indicate to the initiator whether it is to supply data or receive data in response to a previously queued request.

Driven A_GNT# is asserted off the rising edge of SYSCLK in response to an A_REQ#. A reset forces A_GNT# to be negated.

4.4.7 A_IRDY# (Initiator Ready)

Bidirectional

Summary

As a target, the AMD-751 system controller samples A_IRDY# to look for the beginning of a write transfer from the initiator to determine if the initiator is ready to transfer a block. For an AGP write transfer, all data in the given transaction is sent without wait-states, so A_IRDY# only needs to be sampled once for the entire transaction. An AGP read transfer can have wait-states, so the AMD-751 must sample A_IRDY# asserted for each block of a read transfer. A block is the amount of data transferred in four SYSCLK cycles—four doublewords in 1x mode and eight doublewords in 2x mode.

As an initiator, the AMD-751 system controller asserts A_IRDY# to signal the AGP device that it is ready to begin a transfer.

Note: *Because A_FRAME# is not used in an AGP transaction, there is no relationship between A_FRAME# and A_IRDY#, as there is in a PCI transaction.*

Driven, Sampled, and Floated

As an Output: The AMD-751 system controller drives A_IRDY# valid off the rising edge of SYSCLK. For AGP transfers, A_IRDY# is asserted for one clock. For PCI transfers, it is driven during the entire transaction.

As an Input: When the AMD-751 system controller is a target, it samples A_IRDY# on the rising edge of SYSCLK. For AGP transfers, A_IRDY# is sampled only at the beginning of a cycle.

A_IRDY# is floated during reset and when there is no initiator driving the bus.

4.4.8 A_PAR (PCI Bus Parity)

Bidirectional

Summary

A_PAR# is used for PCI transfers on the secondary PCI bus. Its function is the same as that of PAR# on the primary PCI bus (see page 26).

A_PAR# is not used during AGP transfers.

4.4.9 A_REQ# (AGP Bus Request)

Input

Summary As the bus arbiter, the AMD-751 system controller monitors A_REQ# to determine if the graphics controller requests access to the AGP bus. If A_REQ# is sampled asserted, the arbiter asserts A_GNT# as soon as the bus is available.

Sampled A_REQ# is sampled on the rising edge of every SYSCLK.

4.4.10 A_SERR# (System Error)

Input

Summary A_SERR# is used for PCI transfers on the secondary PCI bus. It is not used during AGP transfers.

4.4.11 A_STOP# (AGP Bus Stop)

Bidirectional

Summary A_STOP# is used for PCI transfers on the secondary PCI bus. Its function is the same as that of STOP# on the primary PCI bus (see page 28).

A_STOP# is not used during AGP transfers.

4.4.12 A_TRDY# (Target Ready)

Bidirectional

Summary As an AGP target, the AMD-751 system controller asserts A_TRDY# to signal the start of a read or write data block transfer. A block is the amount of data that can be passed in four SYSCLK cycles—four doublewords in 1x mode, eight doublewords in 2x mode. If a transfer is larger than one block, A_TRDY# must be reasserted for each block. Asserting A_TRDY# every four clock cycles completes the transfer without wait states.

As an AGP initiator, the AMD-751 samples A_TRDY# to determine if data is ready to be transferred.

Driven, Sampled and Floated

As an Output: The AMD-751 system controller drives A_TRDY# valid off the rising edge of SYSCLK.

In AGP-multiplexed mode, data remains on the bus until A_TRDY# is asserted. In AGP-demultiplexed mode, A_TRDY# is asserted for one clock for each block transferred.

As an Input: When the AMD-751 system controller is an initiator, it samples A_TRDY# on the rising edge of SYSCLK. For AGP transfers, A_TRDY# is sampled only at block boundaries.

A_TRDY# is floated during reset and when there is no target driving the bus.

4.5 AGP-Only Signals

4.5.1 ADSTB[1:0] (AD Bus Strobe)

Bidirectional

Summary In 2x mode, ADSTB0 provides timing for A_AD[15:0] and ADSTB1 provides timing for A_AD[31:16]. The graphics controller drives the strobes during AGP write operations, and the AMD-751 system controller drives them during AGP read operations. ADSTB[1:0] serves as a source-synchronized strobe when transferring data in demultiplexed mode. This signal is essentially a copy of the clock that is synchronized to the data. This source-synchronized technique minimizes skew between the strobe and data and compensates for propagation delay. In 1x mode, ADSTB[1:0] is ignored while SYSCLK is used.

Driven, and Floated *As an Output:* A_AD[31:0] and ADSTB[1:0] are both synchronous to SYSCLK. When the AMD-751 system controller is an initiator, it uses the rising and falling edges of ADSTB0 to clock data into the target.

As an Input: When the AMD-751 system controller is a target, it uses the rising and falling edges of ADSTB[1:0] to clock data into its internal registers.

ADSTB[1:0] is floated during reset and when there is no device driving the bus.

4.5.2 PIPE# (APG Pipeline)

Input

Summary The assertion of PIPE# indicates the beginning of a new bus cycle. The AMD-751 system controller queues a request from the initiator on each rising clock edge on which it samples PIPE# asserted. When PIPE# is sampled negated, no new requests are queued.

Sampled The AMD-751 system controller samples PIPE# on the rising edge of every SYSCLK.

4.5.3 RBF# (Read Buffer Full)

Input

Summary An AGP initiator asserts RBF# to indicate that its buffers are full. As an AGP target, the AMD-751 system controller cannot commence a low priority data read to the initiator until it samples RBF# negated. RBF# does not apply to high-priority read data.

Sampled The AMD-751 system controller samples RBF# on the rising edge of SYSCLK before initiating a low-priority read data transfer.

4.5.4 SBA[7:0] (Sideband Address Bus)

Input

Summary In AGP demultiplexed mode, the AMD-751 system controller receives address and command signals from SBA[7:0] rather than A_AD[31:0] and A_C/BE[3:0]#. In AGP multiplexed mode, SBA[7:0] are ignored.

Sampled The AMD-751 system controller samples SBA[7:0] using the SBSTB signal. In 1x mode, the rising edge of SYSCLK strobes in the commands on SBA[7:0]. In 2x mode, both edges of SBSTB strobe in commands on SBA[7:0]. An FFh on these signals is a NOP (no operation).

4.5.5 SBSTB (Sideband Strobe)

Input

Summary Sideband strobe is a synchronization clock generated by the AGP initiator for SBA[7:0] in 2x mode. The AMD-751 system controller uses SBSTB to strobe in commands on the SBA bus to its request queue. SBSTB is driven continuously by the graphics device—NOPs are strobed when no command is present.

The AMD-751 strobes in commands on the rising edge of SYSCLK in 1x mode and both rising and falling edges of SBSTB in 2x mode.

4.5.6 ST[2:0] (Status)

Output

Summary As the AGP arbiter, the AMD-751 system controller drives ST[2:0] when it asserts A_GNT# to inform the graphics controller of the type of data being returned, or that the AMD-751 is ready to accept a command.

Driven ST[2:0] are asserted off the rising edge of SYSCLK. Reset forces ST[2:0] to be negated (bus-available state).

4.6 Miscellaneous Signals

4.6.1 ROM_SCK (SROM Clock)

Bidirectional

Summary ROM_SCK drives the CLK pin of the debug SROM. If this signal is pulled High during RESET#, the SROM supplies the SIP packet. If this signal is pulled Low, the SIP packet is generated internal to the AMD-751 system controller.

4.6.2 ROM_SDA (SROM Data)

Bidirectional

Summary ROM_SDA connects to the data pin of the debug SROM.

4.6.3 SCAN_EN# (Scan Enable)

Input

Summary When SCAN_EN# is asserted, the internal scan chains are enabled. Scan chain heads and tails are multiplexed from functional pins.

This signal has an internal pullup resistor.

4.6.4 TRISTATE#

Input

Summary When TRISTATE# is asserted, all outputs are floated and the NAND tree is enabled.

This signal has an internal pullup resistor.

5 Functional Operation

This section details the operation of the AMD-751 system controller.

5.1 System Addressing

Overview

The AMD-751 system controller supports the AMD Athlon system bus specification. The AMD Athlon processor contains mapping logic for all legacy x86 addresses through an address map (see Table 7 on page 46). As shown in Figure 5, legacy x86 (IBM PC-AT) memory mappings are implemented on the AMD Athlon processor.

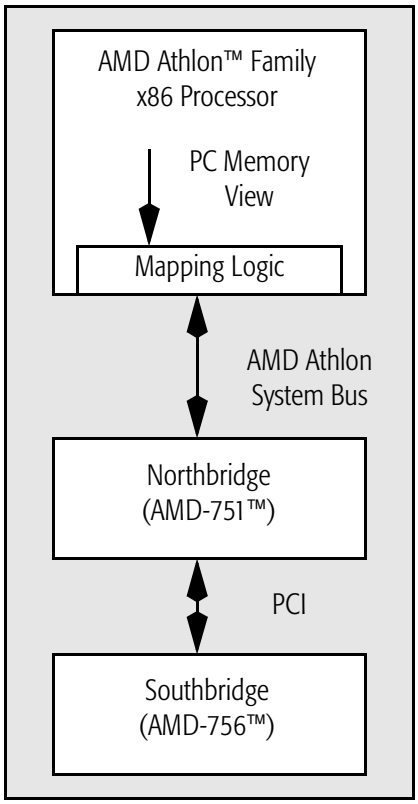


Figure 5. System Memory View

Address Map

Table 7 shows the AMD-751 system controller address map.

Table 7. AMD-751™ System Controller Memory Address Map

Address Space Start	Address Space End	Name/Command	Description
PA msb =0 and 1 FF00 0000	PA msb =0 and 3 FFFF FFFF	Reserved (Masked)	Reserved for use by the AMD-751 system controller.
PA msb =0 and 1 FE00 0000	PA msb =0 and 1 FEFF FFFF	PCI Configuration Space (Masked)	This space is used to create PCI configuration cycles using WrBytes, WrLWs, RdBytes, and RdLWs commands only. See "PCI Configuration" on page 79.
PA msb =0 and 1 FC00 0000	PA msb =0 and 1 FDFF FFFF	PCI I/O Space (Masked)	This space is used to create PCI I/O cycles using WrBytesWrLWs, RdBytes, and RdLWs commands only.
PA msb =0 and 1 F800 0000	PA msb =0 and 1 FBFF FFFF	PCI IACK/Special Cycle Generation (Masked)	WrLWs commands to this space are used to create PCI special cycles. The lower 32 bits of the data are passed on to the PCI bus as both the address and data with the special-cycle PCI command. See Table 8 on page 48 for all special cycles generated by the processor. RdBytes commands to this space are used to create PCI IACK. The lower 16 bits of these addresses are passed on to the PCI unmodified with the IACK PCI command. See "PCI Configuration Accesses" on page 50.
PA msb =0 and 1 0000 0000	PA msb =0 and 1 F7FF FFFF	Reserved (Masked)	Reserved for use by the AMD-751.
PA msb =0 and 0 0000 0000	PA msb =0 and 0 FFFF FFFF	PCI Memory Space (Masked)	The lower 32-bits of these addresses are forwarded, unmodified, to the PCI and are accessed with Wr/RdBytes, Wr/RdLWs, or Wr/RdQWs only. The AMD-751 generates low-order address bits required by the AMD Athlon system bus MASK field.
PA msb =1 and 0 0000 0000	PA msb =1 and 3 FFFF FFFF	Normal Memory (Masked Writes)	DRAM, accessed with masked write commands WrBytes, WrLWs, and WrQWs only.
PA msb =1 and 0 0000 0000	PA msb =1 and 3 FFFF FFFF	Reserved (Masked Reads)	The AMD-751 does not support masked reads to this address space.
PA msb =1 and 0 FF000 0000	PA msb =1 and 3 FFFF FFFF	Reserved (Blocks)	This address space can be used by the AMD-751 for undefined purposes.
PA msb = 0 and 0 0000 0000	PA msb = 0 and 3 FFFF FFFF	Normal Memory (Blocks)	DRAM, accessed with read and write block commands. ***Note:*** *The AMD-751 only uses 32 address bits internally and the address space wraps. Address 1 0000 0000 is treated the same as 0 0000 0000.*

Note:
msb = Most Significant Bit

Figure 6 shows the x86 view of memory from the perspective of the AMD Athlon processor, and mapping to the AMD Athlon system bus memory map.

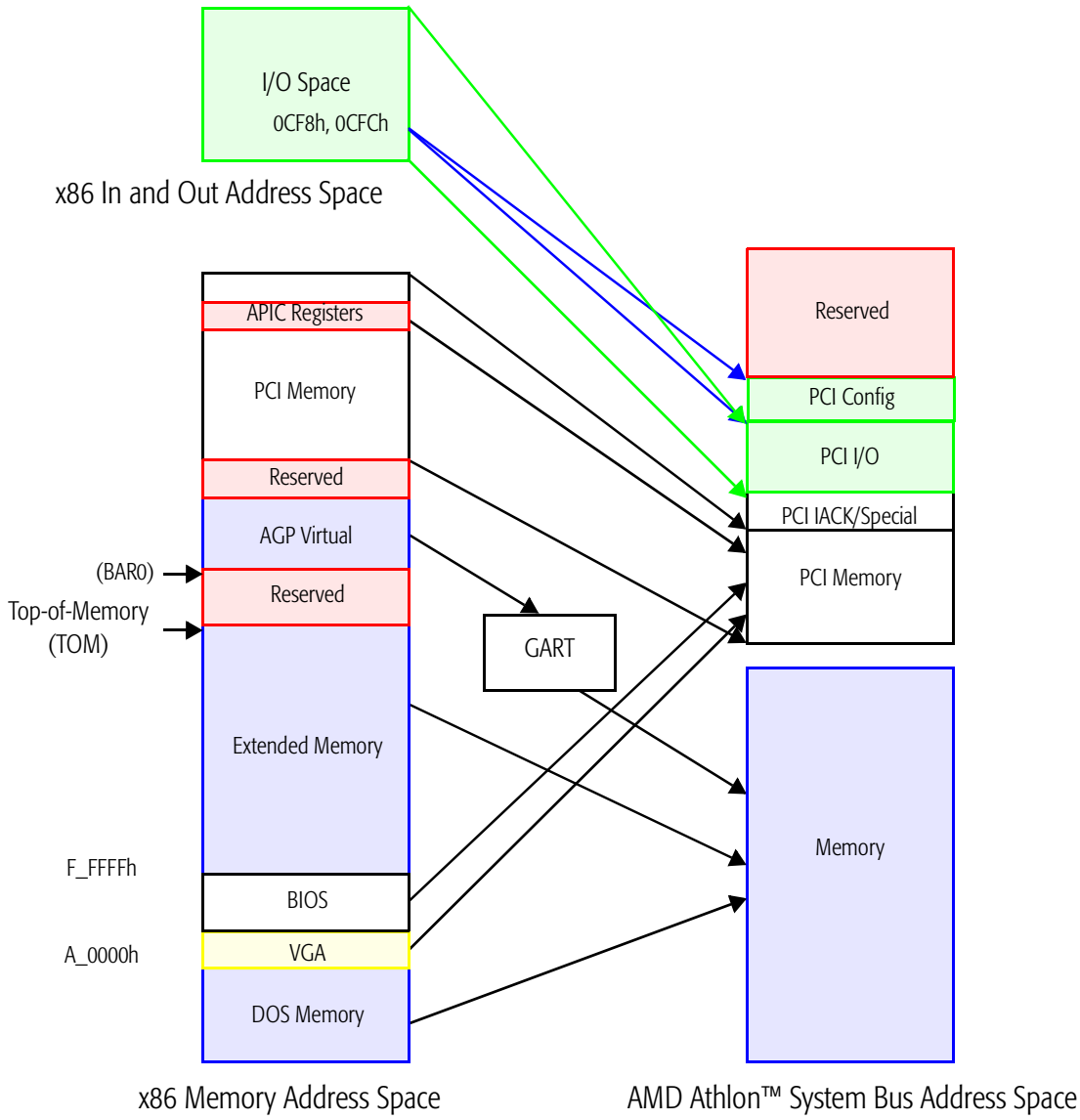


Figure 6. Address Mapping for x86 Legacy

Special Cycles

There are seven special cycles generated by the AMD Athlon processor that are passed onto the PCI bus with specific values in the address and data fields of the PCI special cycle command. Table 8 defines these values (same value for address and data).

Table 8. AMD Athlon™ Processor Special Cycle Encoding

Special Cycle	PCI Address and Data Field Contents	Processor Description	AMD-751™ and AMD-756™ Description
Shutdown	0000 0000	The AMD Athlon generates this special cycle in response to a shutdown condition. The AMD Athlon system bus issues a WrLWs command with PA = SpecCycBase and SDATA[31:0] = 0000_0000h. **Note:** SpecCycBase is msb=0 and PA[33:0] = 1 F800_0000h.	The AMD-751 forwards onto the PCI bus a PCI special cycle command with AD[31:0] = 0000_0000h (address and data). The AMD-756 asserts INIT to the processor.
Halt	0000 0001	The AMD Athlon generates this special cycle in response to a HALT instruction. The AMD Athlon system bus issues a WrLWs command with PA = SpecCycBase and SDATA[31:0] = 0000_0001h.	The AMD-751 waits for all queues to memory to be empty (assumes the PCI grant-enable register is clear, device 0, offset 84). The AMD-751 optionally (through offset 60, bit 18) initiates an AMD Athlon system bus disconnect to the processor. The AMD-751 forwards onto the PCI bus (after the optional AMD Athlon system bus disconnect) a PCI special cycle command with AD[31:0] = 0000_0001h (address and data). The AMD-756 ignores this cycle.
WB Invalidate	0001 0002	The AMD Athlon generates this special cycle in response to executing a WBINV instruction. The AMD Athlon system bus issues a WrLWs command with PA = SpecCycBase and SDATA[31:0] = 0001_0002h.	The AMD-751 forwards a PCI special cycle command onto the PCI bus with AD[31:0] = 0001_0002h (address and data). The AMD-756 ignores this cycle.

Table 8. AMD Athlon™ Processor Special Cycle Encoding (Continued)

Special Cycle	PCI Address and Data Field Contents	Processor Description	AMD-751™ and AMD-756™ Description
Invalidate	0002 0002	The AMD Athlon generates this special cycle in response to executing an INVD instruction. The AMD Athlon system bus issues a WrLWs command with PA = SpecCycBase and SDATA[31:0] = 0002_0002h.	The AMD-751 forwards a PCI special cycle command onto the PCI bus with AD[31:0] = 0002_0002h (address and data). The AMD-756 ignores this cycle.
Flush Ack	0003 0002	The AMD Athlon generates this special cycle in response to assertion of the FLUSH pin after all caches have been flushed to memory. The AMD Athlon system bus issues a WrLWs command with PA = SpecCycBase and SDATA[31:0] = 0003_0002h.	The AMD-751 forwards a PCI special cycle command onto the PCI bus with AD[31:0] = 0003_0002h (address and data). The AMD-756 ignores this cycle.
Connect	0004 0002	The AMD Athlon generates this special cycle as the first cycle after a Stop Grant or Halt system bus special cycle. The Connect cycle is issued by the processor regardless of whether a disconnect was achieved. PA = SpecCycBase and SDATA[31:0] = 0004_0002h.	The AMD-751 forwards a PCI special cycle command onto the PCI bus with AD[31:0] = 0004_0002h (address and data). The AMD-756 ignores this cycle.
Stop Grant	0012 0002	The AMD Athlon generates this special cycle in response to assertion of STPCLK#. The AMD Athlon system bus issues a WrLWs command PA = SpecCycBase and SDATA[31:0] = 0012_0002h.	The AMD-751 waits for all queues to memory to be empty (assumes the PCI Grant-Enable register is clear, device 0, offset 84). The AMD-751 optionally (through device 0, offset 60, bit 17) initiates an AMD Athlon system bus disconnect to the processor. The AMD-751 forwards onto the PCI bus (after the optional AMD Athlon system bus disconnect) a PCI special cycle command—AD[31:0] = 0012 0002 (address and data). The AMD-756 receives and enters the appropriate power state. The AMD-756 can then assert DCSTOP# to the AMD-751 to signal that it should deassert MCKE to the SDRAMs and stop its internal clocks.

PCI Configuration Accesses

In legacy x86 PC systems, PCI configuration cycles are generated by an indirect method. A configuration address register defined at I/O address 0CF8h allows the software to load a 24-bit value that is asserted on the PCI address lines during the next configuration read/write cycle. A configuration data register defined at I/O address 0CFCh allows the software to generate configuration read and write cycles on the PCI using IN and OUT instructions.

Data sent to the configuration data register during OUT instructions is driven on the PCI data lines during the configuration write transaction. Data received in response to a configuration read transaction is returned to satisfy the IN from the configuration data register.

In AMD Athlon system bus systems, PCI configuration cycles are generated by explicitly using RdBytes/RdLWs and WrBytes/WrLWs commands to a 16-Mbyte region at address 1F-E000-0000h, as shown in Figure 6 on page 47. The x86 processor must detect IN and OUT instructions that reference 0CF8h and 0CFCh, and generate the appropriate RdBytes/Rd/LWs and WrBytes/WrLWs AMD Athlon system bus commands.

Command Address Decoding

Decoding logic in the AMD-751 processor and PCI interfaces provides a consistent view of memory and PCI devices.

The AMD-751 considers the processor's request and Physical Address (PA) fields when decoding a command. This command address decoding is summarized as follows:

- If PA msb = 0 and the command is a block command, DRAM is accessed.
  - If PA[31:0] falls between device 0, BAR0 and device 0, BAR0+Len, the address to AGP virtual address space is passed through the GART before presentation to the DRAM.
- If PA msb = 1 and the command is a masked write command (WrQWs, WrLWs, WrBytes), DRAM is accessed.
  - If PA[31:0] falls between device 0, BAR0 and device 0, BAR0+Len, the address to AGP virtual address space is passed through the GART before presentation to the DRAM.

- If PA msb = 0, PA[35:32] = 0, and the command is a masked command, a PCI memory-mapped I/O cycle is performed.
  - Using device 0, offset 14h, BAR1, the access is directed to AMD-751 memory mapped GART control registers (see Chapter 7, "Configuration Registers" on page 123).
  - Using device 1, offset 20h and device 1, offset 22h, memory base and limit registers, the access is directed to either PCI or AGP/PCI using address bits 31–0.
- If PA msb = 0, PA[35:24] = 1F8h, and the command is RdBytes, an IACK special cycle is generated on the primary PCI bus. PA[15:0] are driven on the PCI AD[15:0] bus during this cycle. The data returned on the PCI bus is returned to the processor.
- If PA msb = 0, PA[35:24] = 1F8h, and the command is WrBytes, a PCI special cycle is generated on the primary PCI bus. PA[15:0] are asserted on the PCI AD[15:0] lines during this cycle.
- If PA msb = 0, PA[35:24] = 1FCh or 1FDh, and the command is RdBytes or WrBytes, a PCI I/O command is generated. PA[23:0] are driven on the PCI AD[23:0] lines with the PCI I/O read or write command.
  - Using device 1, offset 1Ch and device 1, offset 1Dh, I/O base and range registers, the access is directed to either the primary PCI bus or the secondary PCI bus.
- If PA msb = 0, PA[35:24] = 1FEh, and the command is RdBytes or WrBytes, a PCI configuration command is generated. PA[23:0] are asserted on the PCI AD[23:0] lines with the PCI configuration read or write command.

  Note: *The low-order processor address bits of PA only go down to physical address PA[3]. For mask operations, the MASK[7:0] bits are encoded to logically create PA[2:0].*

PCI/AGP Master Address Decoding

To route a transaction, the PCI controllers in the AMD-751 system controller compare the received PCI/AGP (secondary PCI bus) address with the BAR registers and the memory configuration registers. In addition, the AMD-751 decodes the AMD Athlon processor commands to properly direct PCI traffic that references the legacy 640-Kbyte to 1-Mbyte memory range. This decoding is summarized as follows:

- If AD[31:0] is less than the physical top-of-memory (from the memory controller), DRAM is accessed.
- If AD[31:0] is above the physical top-of-memory and falls between device 0, BAR0 and device 0, BAR0+Len, the address to the AGP virtual address space needs to pass through the GART before presentation to DRAM.
- If AD[31:0] is above the physical top-of-memory and falls between device 1, 30h memory range decoding register start and ending fields, the secondary PCI bus is accessed (for writes only from the primary PCI).
- Otherwise, the primary PCI bus is accessed (for writes from the AGP/PCI bus only).

  Note: *The AMD-751 does not allow access to the memory-mapped GART control registers from either PCI or AGP/PCI masters. For more information about the GART, see "GART Cache Operation" on page 98.*

Configuration Register Access

The AMD-751 system controller implements most registers as PCI configuration registers. Configuration accesses in the AMD-751 conform to the following rules:

- The AMD-751 is defined to be device 0 and device 1. All external PCI devices must be wired to one of the AD[31:13] wires. Logically, AD[12:11] are assigned to devices 0 and 1 in the AMD-751 system controller.
- Device 0 accesses correspond to the processor-to-PCI bridge registers defined in Chapter 7, "Configuration Registers" on page 123.
- Device 1 accesses correspond to the PCI-to-PCI bridge registers defined in Chapter 7, "Configuration Registers" on page 123.
- Accesses can have a byte, word, or doubleword length and must be naturally aligned.

5.2 Processor Interface

This section describes the interface logic between the AMD Athlon processor and the AMD-751 system controller.

5.2.1 Bus Interface Unit (BIU)

The bus interface unit (BIU) is the interface between the processor and the rest of the system. The BIU receives commands and probe responses from the processor and issues probes to the processor. The BIU initiates all data movement into and out of the processor. Figure 7 shows a BIU block diagram.

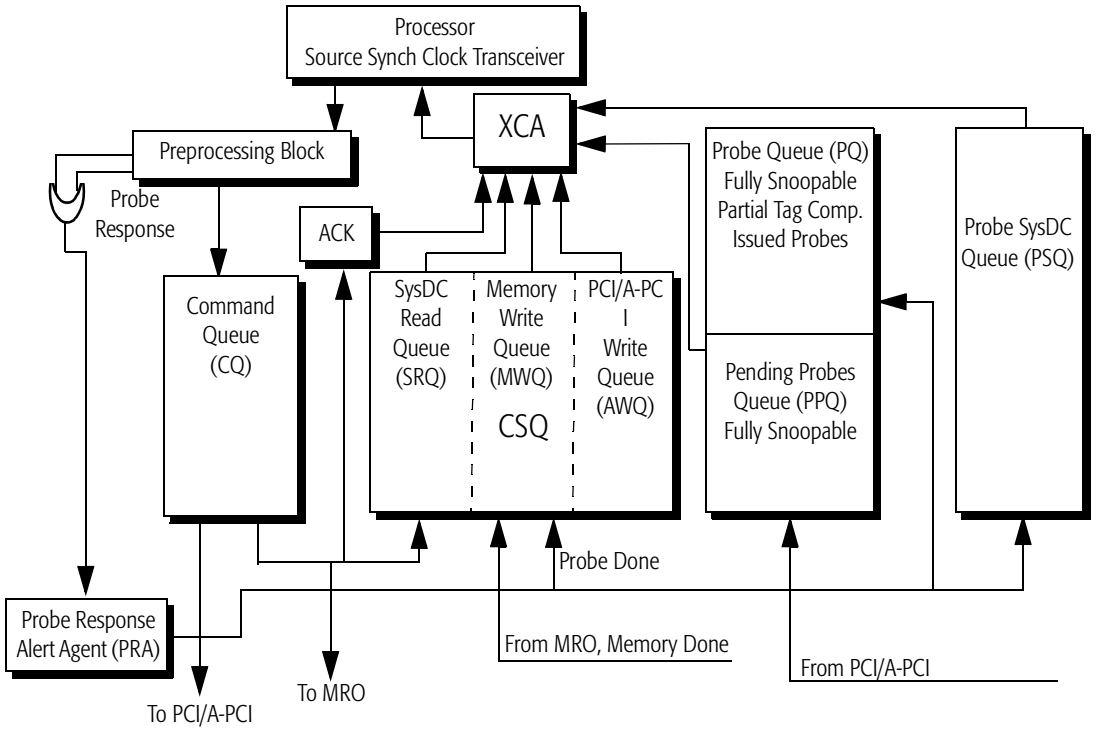


Figure 7. Block Diagram of the Bus Interface Unit (BIU)

BIU Queues

The BIU contains the following queues:

- The command queue (CQ) receives transaction requests from the processor and stores them until they can be dispatched by the destination-dispatch agent.

- The probe queue (PQ) stores probes from the system to the processor. To maintain coherency, the PQ is snoopable.
- The processor system data and control queue (CSQ) stores system data control commands in three separate read and write buffers for data movement in and out of the processor caused by commands generated by the processor itself.
- The probe system data and control queue (PSQ) stores system data control commands for data movement in and out of the processor for probes generated by the system.

BIU Functional Units

The BIU contains the following functional units:

- The probe response alert agent (PRA) broadcasts probe responses it receives from the processor. The probe response can come as a quick probe miss or no-data-movement-required commands, or it can come as a long probe-response command.
- The transaction combiner agent (XCA) is responsible for creating a command packet from the system to the processor containing SysAddOut command format and probe information. The XCA intelligently combines, when possible, the CSQ or PSQ entry and the PQ entry, and transmits it to the processor using the four-cycle SysAddOut command format. When there is either no PQ entry, CSQ entry, or PSQ entry ready for dispatching, a NOP is inserted by the combiner logic. The acknowledge (A-bit) information is also packed in the four-cycle SysAddOut command format.

5.2.2 BIU Start-Up

The AMD Athlon system bus is a unique, source-synchronous, channel that uses protocol and fixed delivery windows to provide maximum performance.

An AMD Athlon system bus is synchronous. However, the use of multiple PLLs in the system and the use of source-synchronous clocking create different clock domains from the processor to the system logic and from the processor to a backside L2 cache. A clock domain is the component or set of components running on one clock signal for its logic operation. For example, the AMD-751 system controller is one clock domain and operates on its own PLL. Although this PLL is driven from the same clock generator as the rest of the system, drifts and skews in the

internal clock place this device in a different clock domain than the processor. Similarly, the processor has its own PLL and, while synchronous, its own clock domain.

When the processor and system logic transfer data back and forth, they send a source-synchronous clock with the data. In this way, the data can be received into input buffers using a clock that has a known, fixed relationship to the data. When data is received, special logic (FIFOs, counters, etc.) allows the data to be reliably moved from the clock domain of the transmitting device to the clock domain of the receiving device. To ensure efficient, reliable operation, and to know which clock edge has which data, this logic must be programmed for the component and board delays before any transfer can occur.

The processor uses a packet-based protocol with predefined delays from protocol packets to data transfers. However, these delays are defined based on the processor clock frequency and certain programmable values. These values must be correctly programmed and agreed upon before any transfer can occur.

As part of the reset sequencing, the processor and system logic use a set of shared interface pins (CONNECT, CLKFWDRST, and PROCRDY) to serially transfer a serial initialization packet (SIP) from a ROM table in the AMD-751 to the processor. Resister strapping options on the AMD Athlon system bus card-edge connector select the entry in this ROM table. The strapping tells the AMD-751 what speed and what processor type is in the processor module. For the appropriate entry in the table, the AMD-751 transmits a serial bit stream to the processor and uses other bits for its own state machines and logic. In this way, the processor and the AMD-751 establish a predefined set of operating assumptions and conditions.

Because the AMD Athlon system bus protocol is packet-based, the beginning of each packet must be negotiated between the sender and the receiver. This negotiation is accomplished by starting with an all 1b bit pattern (a NOP command) until the first non-NOP packet boundary is identified. From that point forward, simple counters can track the start of each packet. Initially the processor issues a packet to the AMD-751, which marks the beginning of the packet. The AMD-751 responds with a packet that the processor uses to synchronize the return path. As long as the bus clocks continue to run, the packet-timing relationship remains valid.

Serial Initialization Packet (SIP) Protocol

The SIP protocol is shown in Figure 8 and described in Table 9. For a typical system reset sequence, the AMD-756 peripheral bus controller asserts PCIRST# to the system reset input and CPURST# to the processor RESET# input.

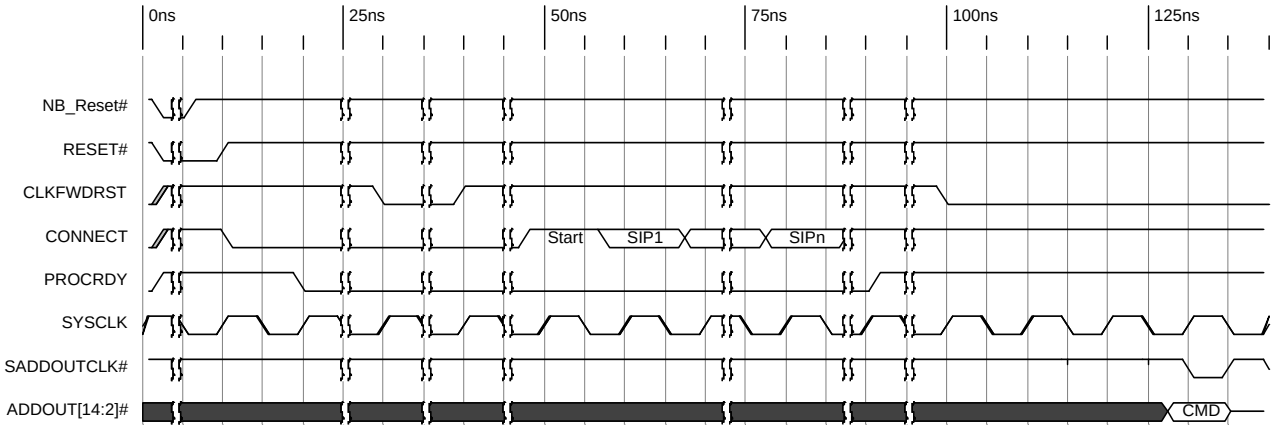


Figure 8. SIP Protocol

Table 9. SIP Protocol States and Actions

State	Action
1	When NB_RESET# and RESET# are asserted, the system asserts CONNECT and CLKFWDRST and the processor asserts PROCRDY.
2	When NB_RESET# is deasserted, the system deasserts CONNECT, but continues to assert CLKFWDRST. When RESET# is deasserted, the processor deasserts PROCRDY and is ready for initialization (through the SIP protocol). ***Note**: The system must be out of reset before the processor deasserts PROCRDY.*
3	One or more SYSCLK periods after the deassertion of PROCRDY, the system deasserts CLKFWDRST. (States 3 and 4 are performed for AMD Athlon system bus legacy reasons.)
4	One or more SYSCLK periods after the deassertion of CLKFWDRST, the system again asserts CLKFWDRST.
5	Either at the assertion of CLKFWDRST or one or more SYSCLK periods later, the processor expects the *start* bit (CONNECT asserted) of the SIP. The system delivers the SIP containing the processor source-synchronous initialization state over CONNECT. After the SIP is transferred, the system asserts and holds CONNECT, which indicates the end of the SIP transfer to the processor.
6	One or more SYSCLK periods after receiving the SIP, the processor asserts PROCRDY to indicate to the system that it has received the SIP, initialized itself, and is ready.

Table 9. SIP Protocol States and Actions (Continued)

State	Action
7	One or more SYSCLK periods after the assertion of PROCRDY, the system deasserts CLKFWDRST.
8	Three SYSCLK periods after CLKFWDRST deassertion, the processor drives its source-synchronous clocks. The processor indicates bit-time 0 to the system by issuing a non-NOP command on the appropriate source-synchronous clock.

AMD Athlon™ Processor SIP Mapping. The AMD-751 system controller is responsible for supplying initialization values to the AMD Athlon processor that are a function of physical AMD Athlon system bus length, SYSCLK frequency, and processor clock multiplier. These values must be loaded prior to any AMD Athlon system bus transactions and are supplied through the SIP protocol. The AMD-751 implements two modes—production and debug. During reset, if ROM_SCK is pulled High (debug mode), the SROM supplies the SIP packet to the AMD-751. If ROM_SCK is pulled Low (production mode), the SIP packet is generated internally.

5.2.3 Processor Write Posting

The AMD-751 system controller contains two write buffers to enhance write performance. Each buffer can hold four entire cache lines, also referred to as data blocks. Each data block is 64 bytes (eight quadwords). The write buffers are always enabled. The memory controller supports both single writes and block writes. Block writes are more common in a typical system than single writes because the processor uses writeback caches, which transfer data in blocks. When a writeback cache is employed, the AMD-751 sees a block transaction every time the processor clears a cache line. The posted write buffers of the AMD-751 can handle four back-to-back block transactions without wait states. Figure 9 on page 58 shows the organization of the posted write buffers.

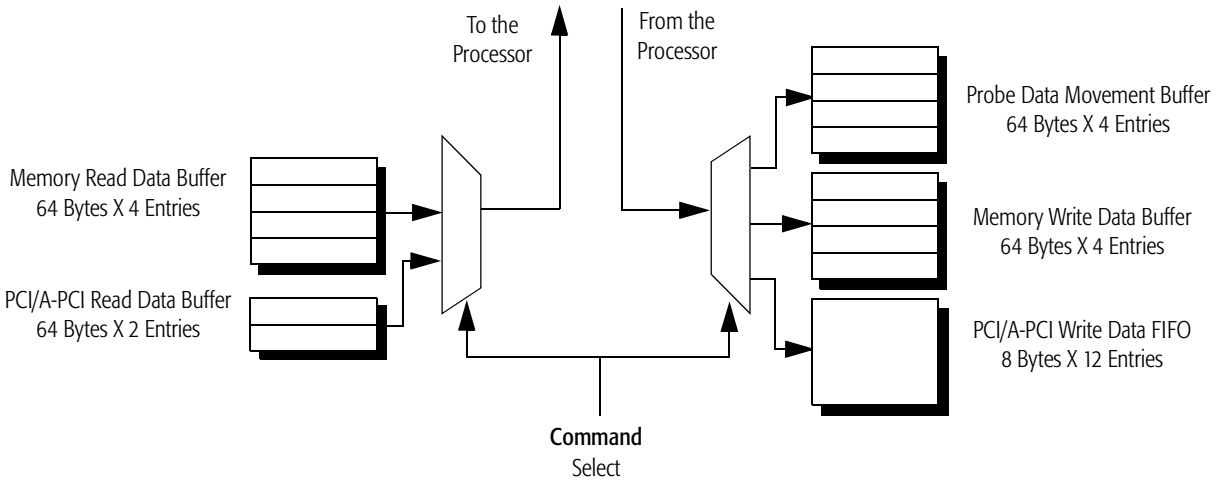


Figure 9. AMD Athlon™ System Bus Data Buffers (BIU)

The write buffers are organized as pseudo first-in-first-out (FIFO) buffers. That is, writes from the buffers to memory are usually performed in the order they are received from the processor. Four consecutive write transactions, whether single or block, fill all four 64-byte buffers. Write buffers continue to accept data until either the buffers are full or all data from the processor is received. At that point, the AMD-751 begins writing data to the DRAM. As each pending write to main memory is performed, freeing the corresponding buffer, the memory controller sends a command to the processor.

5.2.4 Read Buffer

The AMD-751 system controller contains two, 64-byte by four-entry read buffers. Each buffer can hold an entire block of data. Memory reads that fill the processor caches are by far the most common types of reads. These reads occur as a burst read of eight quadwords (64 bytes).

The read buffers snoop write transactions to maintain data coherency. If a write transaction occurs to an address where one of the read buffers contains data, that read buffer is invalidated.

5.3 Memory Interface

The AMD-751 system controller memory interface contains two functional blocks—the memory request organizer (MRO), which serves as a data crossbar and kernel for the AMD-751, and the memory controller (MCT), which is designed to operate up to three PC-100 SDRAM DIMMs.

5.3.1 Memory Request Organizer (MRO)

The memory request organizer (MRO) is responsible for scheduling read/write requests to main memory from the BIU, primary PCI, and secondary A-PCI (AGP). The MRO evaluates all the dependencies a particular read/write request may have, waits for all these dependencies to resolve, and routes the data accordingly.

The MRO consists of the following modules:

- Memory queue arbiter (MQA)
- Four memory read queues (MRQ[3:0])
- Memory write queue (MWQ)
- Memory write selector (MWS)

A top-level diagram of the MRO is shown in Figure 10 on page 60.

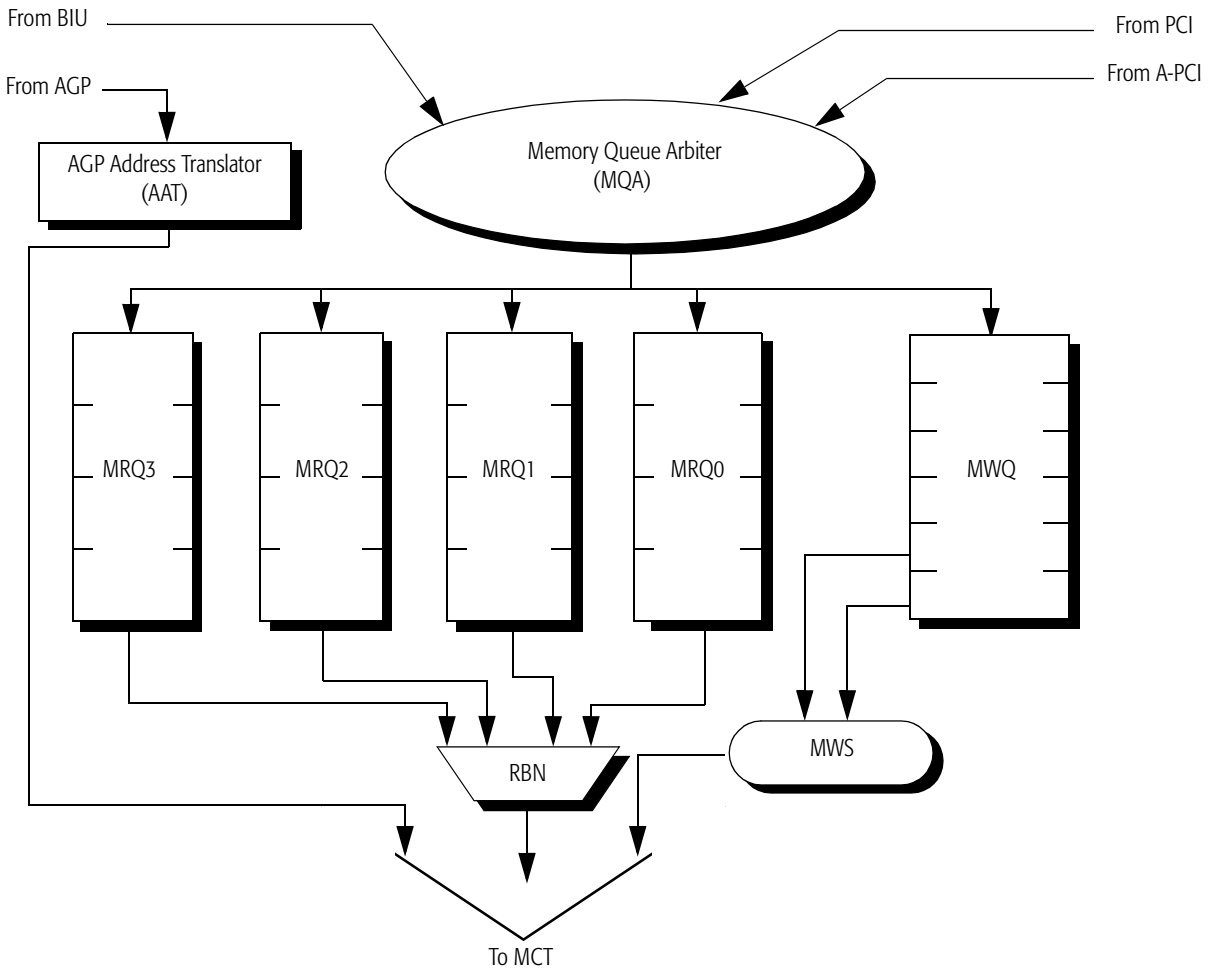


Figure 10. Memory Request Organizer (MRO) Block Diagram

Memory Queue Arbiter (MQA)

The memory queue arbiter (MQA) is responsible for choosing between read and write requests from all sources (BIU, PCI, and A-PCI) in a round-robin (RBN) manner. The MQA sends one read or write transaction to the MRQs or MWQ on each clock cycle. In addition, the arbiter performs translation from the physical address to the DRAM bank/row/column address, based on the DRAM socket addressed in a request.

A two-level prioritization scheme is used. At the highest level there are two requesters—the BIU and all other requesters OR'ed together. The second level of the hierarchy contains a round-robin arbiter between the peripheral requesters. Figure 11 on page 61 shows the structure of this arbiter. AGP requests undergo address translation in the MRO and are forwarded directly to the MCT.

The output from the MQA is passed on to one of the MRQs or the MWQ, to be scheduled by the memory request scheduler (MRS) as described in the "Memory Controller (MCT)" on page 63. The MRS is responsible for scheduling requests from various sources onto the actual memory interface.

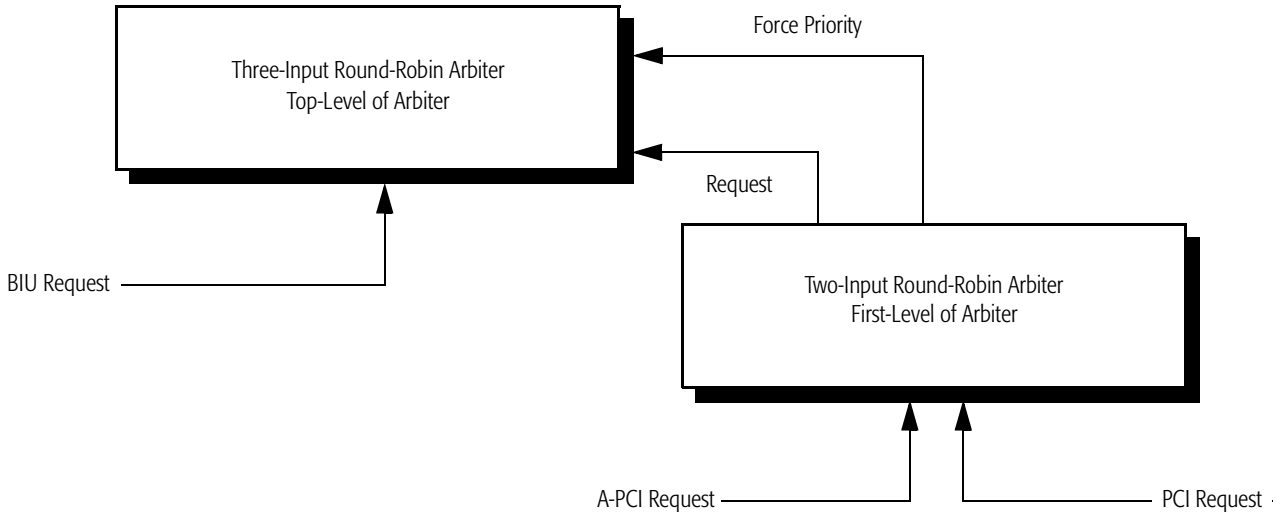


Figure 11. Memory Queue Arbiter (MQA) Block Diagram

The arbiter is disabled if there are no free entries in the MRQs or MWQ. All requests are held until some of the older requests in the full queue are serviced. However, if one of the queues has available entries, the arbiter continues to issue requests to it, even if the other queue is stalled.

The Memory Read Queues (MRQ)

The four memory read queues (MRQ) store four read requests, each directed to the main memory (with the exception of AGP read requests, which bypass the read queue). Each MRQ holds read requests for one of the four banks of memory. Each entry contains transfer-relevant information, such as address and size, as well as dependency flags. The flags are cleared when the dependencies are removed.

A read-request entry is placed in the MRQ by the MQA. The new request is entered on top of the latest request in the queue, unless the request is a page hit (PH). In the case of a page hit, the request is placed ahead of any page-miss requests, but behind any older page-hit requests. Therefore, the queue is built with the oldest page-hit request at the bottom of the queue and the newest page miss at the top. The RBN schedules the read request to the MCT in a round-robin manner.

When the entry is put into the MRQ, the address of the read request is passed through the memory write queue (MWQ) and compared with all valid MWQ entries. If one or more write requests in the MWQ are pending to the same cache line addressed by the read request, a dependency exists and this particular read request cannot be scheduled by the MRS until the writes have completed.

Memory Write Queue (MWQ)

The memory write queue (MWQ) stores six write requests directed to main memory. Each entry contains transfer-relevant information, such as address and size, as well as dependency flags. The flags are cleared when the dependencies are removed.

When the entry is put into the MWQ, the address of the write request is compared with all current entries in the MWQ. If one or more write requests in the MWQ are pending to the same cache line addressed by the new write request, the dependent writes are executed in order.

Memory Write Selector (MWS)

The memory write selector (MWS) chooses one eligible write to present to the MCT. The write that is chosen is the oldest entry that has resolved all of its data dependencies. In addition, the module contains logic to correctly sequence a merged write to the MCT, which occurs when a partial cache line write results in a processor probe data movement. The processor data is written to memory first, followed by the partial cache line data. Both writes originate from a single MWQ entry, presented back-to-back by the MWS.

AGP read/write requests are handled in a slightly different manner than the other requests. AGP requests have address translation applied in the MRO, and then the requests are forwarded to the MCT.

The MRO forms a fully-coherent subsystem. To determine any dependencies, all read requests entering the read queue cause a probe to all pending write requests in the write queue. If a dependency is detected, the read is not sent to memory until the write is serviced. Likewise, all write requests entering the write queue are compared with existing entries to see if dependencies exist. If a dependency is found, the dependent writes are executed in order.

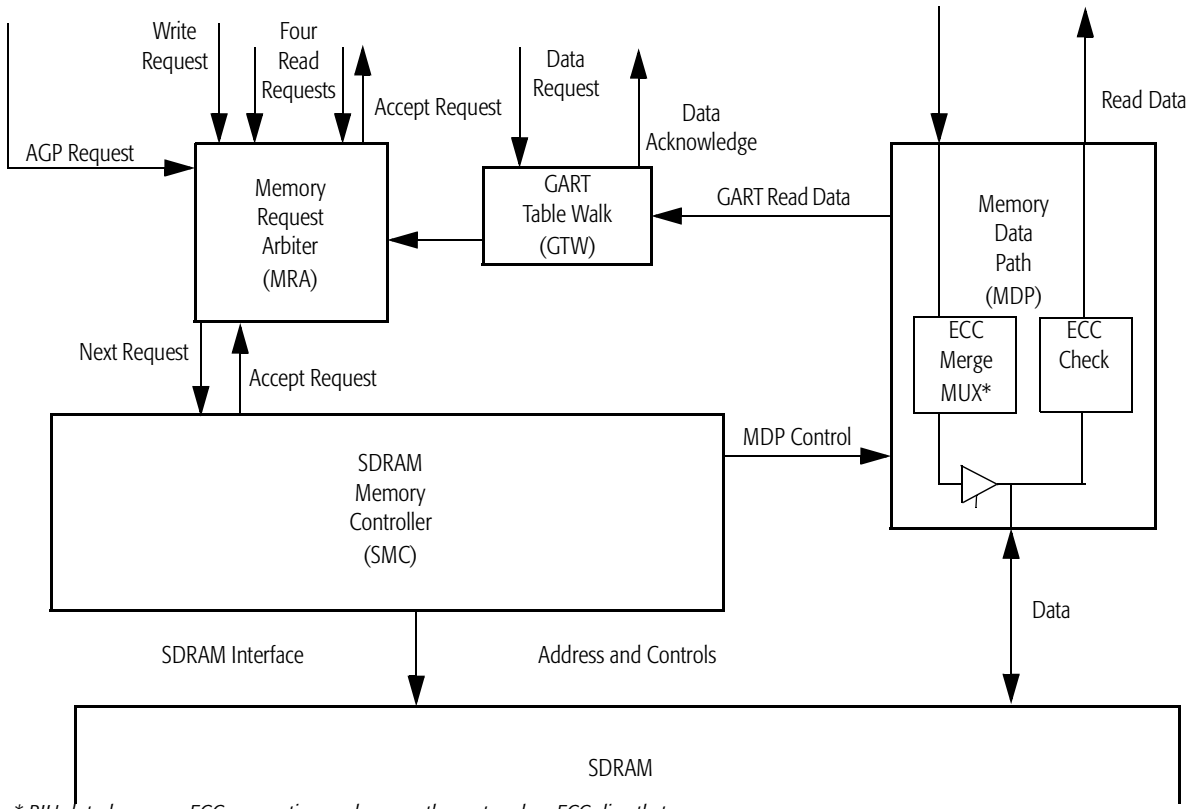
5.3.2 Memory Controller (MCT)

The memory controller (MCT) arbitrates and optimizes incoming memory requests, handles ECC and graphics address remapping table (GART) walks (GTW), gathers and retrieves data, and controls up to three SDRAM modules or six banks.

Bank one is enabled by CS[0]#, bank two is enabled by CS[1]#, and so on. Single-banked memory modules require one CS[5:0]# signal. Dual-banked memory modules occupy two rows of memory and require one SRAS# and two CS[5:0]# signals.

DRAM banks are grouped into three pairs. Each pair can have zero, one, or both banks populated. See Figure 13 on page 67 for more information.

Figure 12 shows the block diagram for the MCT. The MCT configuration registers are described in Chapter 7, "Configuration Registers" on page 123.



Note: ** BIU data bypasses ECC generation and passes the system bus ECC directly to memory.*

Figure 12. Memory Controller (MCT) Block Diagram

MCT Features

The MCT has the following features:

- Support for up to three, 168-pin SDRAM DIMMs using 16-Mbit (with the exception of 32-bit wide devices), 64-Mbit, and 128-Mbit density SDRAMs.
- Support for SDRAM DIMMs with either 72 bits with error correcting code (ECC) or 64 bits with no ECC.
- Support for up to 768 Mbytes of memory (128-Mbit by four technology equals a 256-Mbyte per slot capacity for up to 768 Mbytes).
- Support for up to four open pages within one CS (the device selected by chip select) for one-quadword AGP requests.
- Support for ECC with no scrubbing or correction of memory. ECC from the AMD Athlon system bus is passed directly into memory without checking and regeneration. No support for parity generation and checking is provided.
- Support for only one speed of SDRAM. The MCT does not support a different SCAS# latency for each socket.
- Power-down of the chipset is supported through the SDRAM automatic refresh.
- Automatic refresh of idle slots (attempt to keep refresh from stealing bus utilization).
- The MCT selects the next request to optimize bus utilization as first importance (with configuration registers to limit starvation) and then by the actual importance of the request.
- The MCT tracks up to four open pages and optimizes for up to four open banks within a chip select (CS).

MCT Blocks

The MCT consists of the blocks described in this section.

Memory Request Arbiter (MRA). The MRA arbitrates and optimizes between the different memory requesters—one AGP request, one memory write queue (MWQ) request, four memory read queue (MRQ) requests, and one MCT internal request—from the GART table walk (GTW) address translation engine (ATE). (For more information, see “GART Address Translation Engine (ATE)” on page 100.) The MRA can select one request on each cycle and present it to the SDRAM memory controller (SMC).

SDRAM Memory Controller (SMC). The SMC takes each request presented from the MRA and schedules and optimizes the correct events onto the SDRAM interface. In addition, the SMC

controls traffic and ECC production in the memory data path (MDP), refreshes SDRAM, power-down, and power-up, initializes SDRAM on RESET, and sets the mode register inside the SDRAM with a BIOS-specified value for device 0, offset 5A, bit 7.

Memory Data Path (MDP). The MDP is responsible for providing and distributing data for memory requests and for dealing with ECC and write-merging memory write requests of less than 64-bits that require ECC.

5.3.3 Address Mapping and Memory Organization

Addresses are decoded into the following four controls for SDRAM operation:

- CS (Chip Select)—Three DIMM sockets are supported, each with up to two CS signals (CS[5:0]#). Each CS[5:0]# signal is determined by performing an address less-than comparison across all the end address configuration registers (see Chapter 7, "Configuration Registers" on page 123) and selecting the slot associated with the lowest slot match.
- Bank—Bank selects one of up to four banks within a CS (or memory module selected by CS). The bank signal is encoded in two bits that select either two or four banks within a CS.
- Row—Row selects one of up to 8-Kbyte rows within a bank. Row addresses are up to 13 bits.
- Col—Col selects one of up to 4-Kbyte quadwords within each row. Column addresses are up to 12 bits.

These four parts of an address request are translated and provided by each memory requester (AGP, MWQ, MRQ, and ATE). All signals coming to the MCT are encoded. Using the CS, bank, and row information, the MRA selects the next request for the SMC to handle. The SMC then schedules the correct sequence of events onto the SDRAM interface and merges the bank bits onto the correct row and column bits according to the memory size of the destination, configuration register settings, and SDRAM organization.

The memory organizations listed in Table 10 on page 66 for 16-Mbit and 64-Mbit SDRAM are from current SDRAM specs and from the JEDEC standard.

Table 10. SDRAM Memory Organizations

SDRAM Organization	Number of SDRAMs Needed for 64-Bit Bus	Total Memory Module Size	Number of Bank Bits /Address Bits	Number of Column Bits	Number of Row Bits
16 Mbit					
4-Bit Wide Device Two Banks x 2 Mbytes	16	32 Mbytes	1/MA11	10	11
8-Bit Wide Device Two Banks x 1 Mbyte	8	16 Mbytes	1/MA11	9	11
16-Bit Wide Device Two Banks x 512 Kbytes	4	8 Mbytes	1/MA11	8	11
32-Bit Wide Device Two Banks x 256 Kbytes — Not Supported	2	4 Mbytes	1/MA10	8	10
64 Mbit					
4-Bit Wide Device Four Banks x 4 Mbytes	16	128 Mbytes	2/MA12-13	10	12
Two Banks x 8 Mbytes	16	128 Mbytes	1/MA13	10	13
8-Bit Wide Device Four Banks x 2 Mbytes	8	64 Mbytes	2/MA12-13	9	12
Two Banks x 4 Mbytes	8	64 Mbytes	1/MA13	9	13
16-Bit Wide Device Four Banks x 1 Mbyte	4	32 Mbytes	2/MA12-13	8	12
Two Banks x 2Mbytes	4	32 Mbytes	1/MA13	8	13
32-Bit Wide Device Four Banks x 512 Kbytes — Not Supported	2	16 Mbytes	2/MA11-12	8	11
Two Banks x 1 Mbyte — Not Supported	2	16 Mbytes	1/MA12	8	12
128 Mbit					
4-Bit Wide Device Four Banks x 8 Mbytes	16	256 Mbytes	2/MA12-13	11	12
8-Bit Wide Device Four Banks x 4 Mbytes	8	128 Mbytes	2//MA12-13	10	12
16-Bit Wide Device Four Banks x 2 Mbytes	4	64 Mbytes	2//MA12-13	9	12
32-Bit Wide Device Four Banks x 1 Mbytes	2	32 Mbytes	2/MA12-13	8	12

Note:
Shaded rows indicated unsupported memory sizes.

5.3.4 SDRAM Interface Memory

Figure 13 shows an SDRAM interface example.

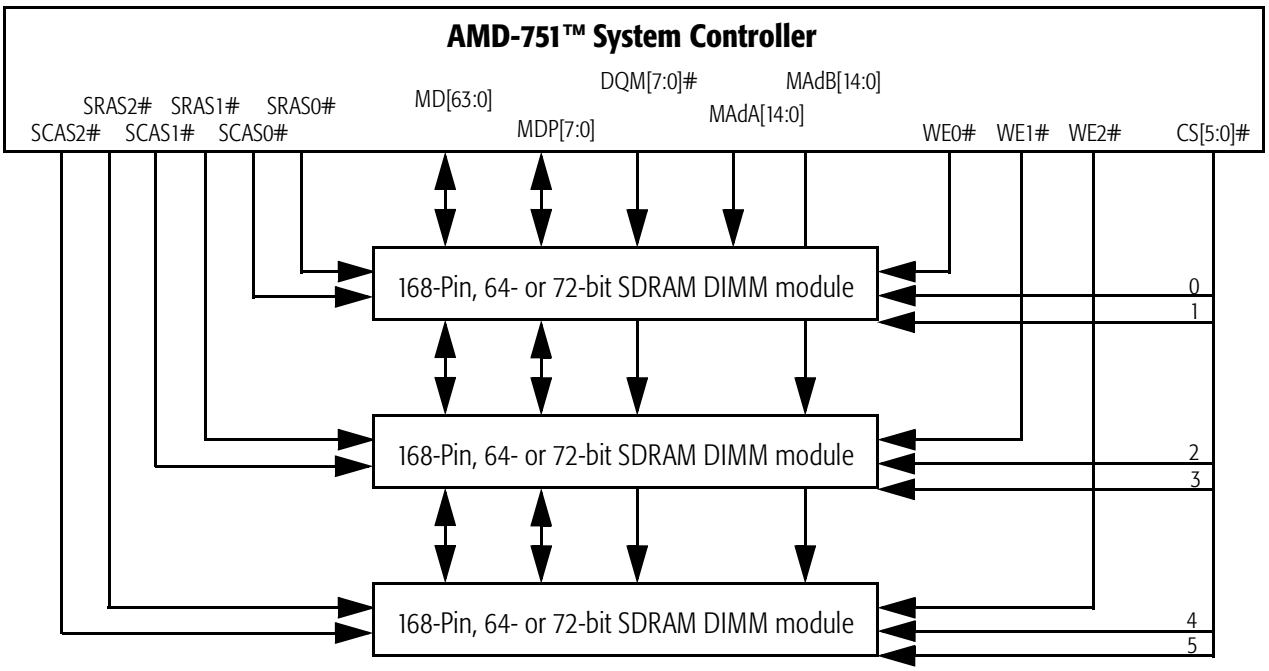


Figure 13. SDRAM Interface Example

Memory Detection

The AMD-751 system controller can accommodate different memory sizes in different slots. To determine the type and size of the memory device, the BIOS can use the serial presence detect (SPD) feature found in PC-100 DIMMs (using the AMD-756 peripheral bus controller to read DRAM information) or a more general-purpose sizing algorithm. See the *AMD Athlon™ BIOS Developers Guide*, order# 21656 for more information.

Error Correcting Code (ECC)

The AMD-751 system controller supports error correcting code (ECC) to check the integrity of transactions with system memory. ECC, also referred to as Hamming code, corrects single-bit and some double-bit errors. The DRAM ECC status register is enabled in device 0, offset 59h–58h (see page 145).

ECC operation requires that system memory be initialized on power-up. In this procedure, the BIOS writes to every memory location, generating valid ECC that is stored in the DRAM parity bits. If this procedure is not performed, errors occur when writing data smaller than a 64-bit quadword.

Data from the AMD Athlon processor includes ECC, which is passed directly into memory—providing protection along the whole data path.

Memory types (72-bit and 64-bit DIMMs) cannot be mixed when ECC is enabled.

DRAM Refresh

The AMD-751 system controller provides DRAM refresh that is transparent to the rest of the system. Normal and burst can be selected through device 0, offset 5Ah–5Bh (see page 145). Accesses to the read and posted write buffers are allowed during a refresh period. DRAM self-refresh mode is entered when the system enters an S1 or S2 ACPI power-down state.

In addition, the AMD-751 system controller contains a refresh counter that provides 4096 refresh cycles on MA[11:0]. The refresh period is derived by dividing MCKE by 512, 1024, 1536, or 2048. The refresh period is programmed in the DRAM Mode/Status register (device 0, offset 5Ah) bits 1–0. Figure 14 shows the DRAM refresh timing.

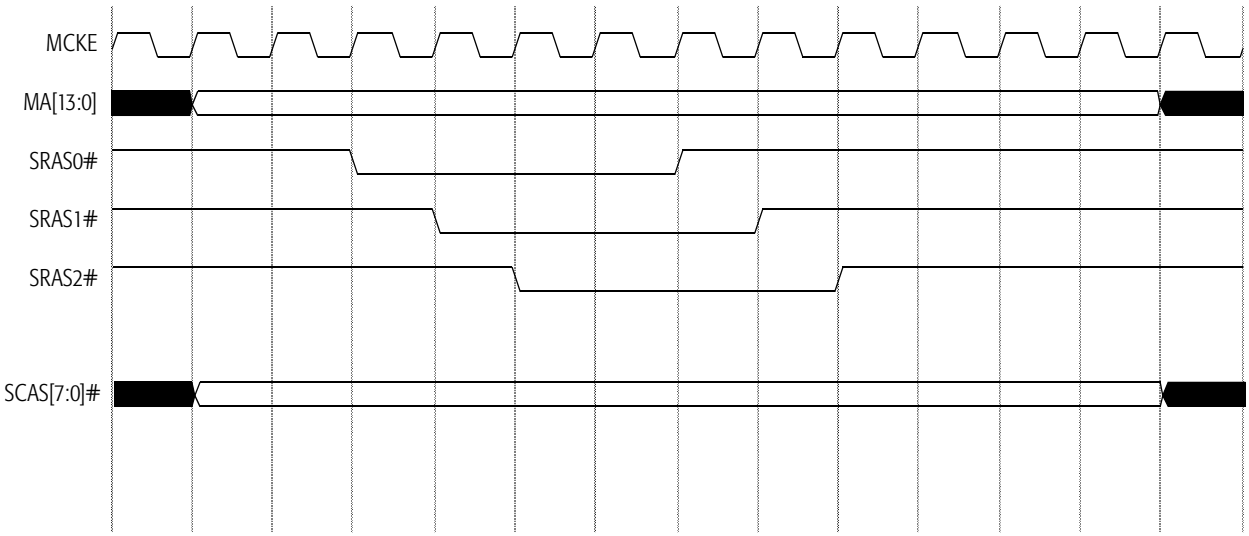


Figure 14. DRAM Refresh Timing

For example, in a system with SYSCLK = 100 MHz and a refresh interval of 1024 cycles every 16 ms, the refresh divisor is calculated as follows:

Refresh Interval/Refresh Cycles ≥ Refresh Cycles • Clock Period

$(16 \times 10^{-3}\text{sec}) / 1536 \text{ cycles} \geq (1536 \text{ cycles}) (10 \times 10^{-9}\text{sec})$

Refresh State Machine

The refresh state machine keeps track of when each of CS[5:0] needs to be refreshed. Each CS is refreshed independently. Refresh is only performed on rows that are populated. A concurrent refresh cycle can be executed in parallel with other read and write requests, if there is no CS conflict and the command bus is free. Figure 15 shows the refresh timers and counters.

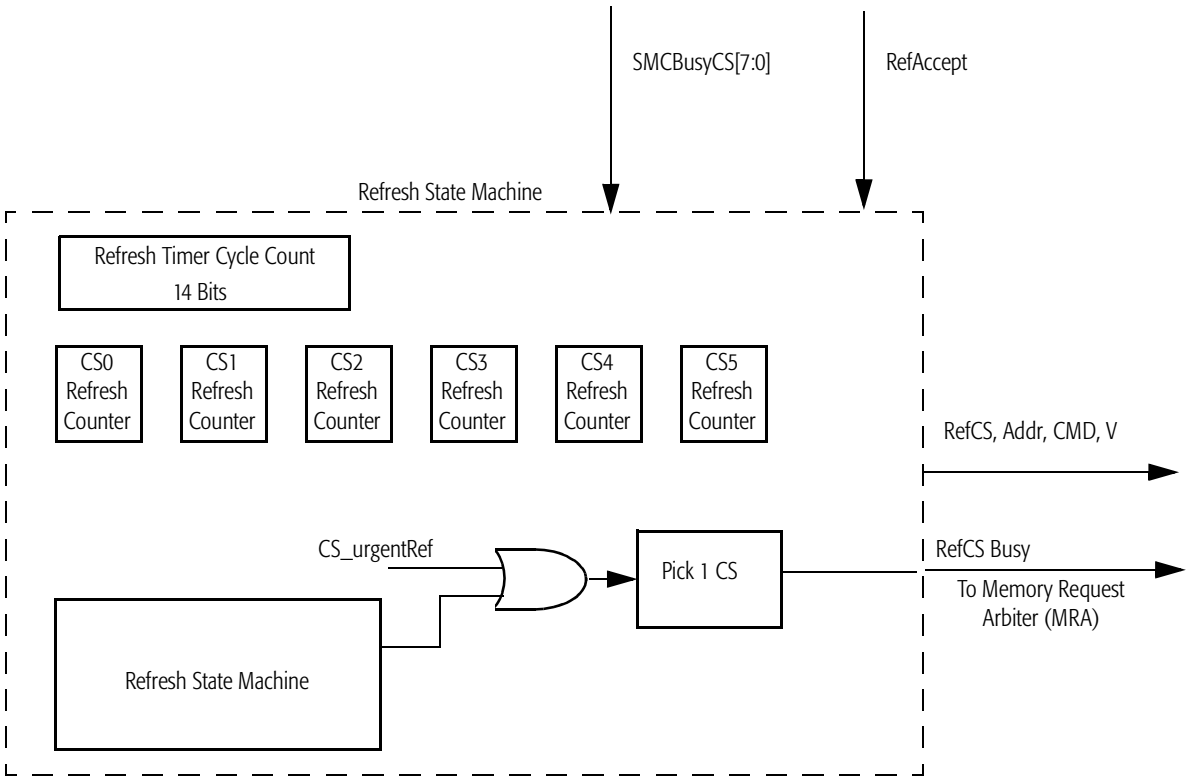


Figure 15. Refresh Timer and Counters

SDRAM Initialization

Initialization can be broken down into two parts. The first is the SDRAM initialization and the second is the BIOS initialization to configure the MCT for correct and optimal operation.

SDRAMs require the following sequence to initialize:

1. Bring up V_{DD} and start the clock (done by external logic).
2. Assert MCKE and DQM inputs High, hold the other inputs at a NOP command—the MCT forces this condition when RESET# is asserted.
3. Wait 100 to 200 microseconds (which is ensured by RESET# staying asserted for this length of time), perform a minimum of eight auto-refresh cycles to all banks by setting the SDRAM initialization bit of the DRAM Mode/Status register (device 0, offset 5Ah, bit 9), and set the refresh counter refresh value (offset 5Ah, bits 1–0) to 11 (see page 146). Then wait until SDRAM initialization status (bit 9) is reset, which indicates that eight refresh cycles have occurred. The BIOS then turns off refresh again by writing a zero into the refresh.
4. Write a 1 to SDRAM operation mode select (offset = 5Ah, bit 7) to issue a mode register set command. The BIOS then needs to write to the address corresponding to the value to which the mode register is set (the mode command is on the address lines and default address mapping is set to 16 Mbits). The conditions should be set as follows:
   - A11–A7 must be equal to 00000b.
   - A6–A4 = 010b for SCAS#=2 or 011b for SCAS#=3.

     SCAS# latencies of 2 or 3 are specified by DIMM manufacturers (see “Synchronous DRAM (SDRAM)” on page 72).
   - A3 = 1 (for interleave burst).
   - A2–A0 = 011b for eight quadword bursts.

Row A11–A0 corresponds to A11, A12, and A22–A13 in 16-Mbyte address mapping. See Table 23 on page 142 for address mappings.

Memory Controller Initialization

To correctly initialize the MCT, the BIOS must perform the following steps:

1. Program DIMM timing values in device 0, offset 54h.
2. Enable the refresh counter (device 0, offset 5Ah, bits 1–0) with a conservative value (for example, 11 = 512 cycles between refreshes).
3. Set the timing configuration registers to the worst case timing of any DIMM.
4. Enable each CS, one at a time, by using the bank-enable registers (device 0, offsets 40h–4Bh) and perform the following steps to determine the size of each CS:
   A. Configure each CS to be a 256-Mbit memory module with a 512-Mbyte ending address.
   B. Write a unique pattern into the topmost quadword of memory (address = 3FF_FFFFh).
   C. Read the location (address = 3FF_FFFFh). If the pattern read is the one written in the previous step, it is a 512-Mbyte module. If not, then:
      i. Write a unique pattern into the topmost quadword of memory (address = 1FF_FFFFh).
      ii. Read the location (address = 1FF_FFFFh). If the pattern read is the pattern written in the previous step, it is a 256-Mbyte module. If not, then:
         * Keep changing the msb to 0 until the size is determined.
   D. Repeat this process for each slot until the number of slots is determined.

5.3.5 Shadow RAM

To prevent altering the content of this crucial system code, the BIOS normally resides in ROM. Because ROM is substantially slower than RAM, most systems provide for copying the ROM contents to the upper memory area of RAM and making that area read-only. The portion of RAM containing the BIOS copy is referred to as shadow RAM.

The AMD-751 system controller does not contain any hardware to support the shadowing of system, video, and other BIOS functions to accelerate access. This capability is supported with the AMD Athlon processor memory type and range registers (MTRR).

5.3.6 Synchronous DRAM (SDRAM)

The AMD-751 system controller only supports synchronous DRAM (SDRAM), which is a cost-effective, mainstream type of system memory. SDRAMs use a clock to synchronize address and data rather than row and column strobes. The net effect is burst performance that approaches SRAM. In addition, SDRAMs can be programmed to select the burst length, write mode, and type of burst (sequential or linear). The PC-100 specification has standardized the characteristics of SDRAM DIMMs. Table 11 shows the timing parameter PC-100 Rev. 1.0 SDRAM DIMM part nomenclature used by manufacturers.

Table 11. PC-100 REV. 1.0 SDRAM DIMM Part Nomenclature

T_{CL}	T_{RCD}	T_{RP}	Comments
2 Clocks	2	2	Lowest Latency
3 Clocks	2	2	
3 Clocks	2	3	
3 Clocks	3	3	Highest Latency

Notes:
T_{CL} is the SCAS# latency.
T_{RCD} is the SRAS# to SCAS# delay.
T_{RP} is the row precharge.

SDRAM memory does not toggle SCAS# to get new data, but simply increases a counter to supply the address for succeeding cycles, which substantially reduces bus delays. The basic characteristics of SDRAM are as follows:

- SRAS# and SCAS# act as clock enables rather than strobes.
- The output drivers remain on when SCAS# is negated. They are turned off when WE[2:0]# or CS# is asserted High or when the burst count expires.
- Read data is valid until the next rising clock edge.
- Write data is sampled on each rising clock edge.
- DQM[7:0]# determine which bytes are read or written.
- Control signals need only be valid during CS#.

The BIOS configures the memory controller for SDRAM memory operation by programming device 0, offset 55h–54h (see page 143).

Multiple Pages Open

Using SDRAM, the AMD-751 system controller allows multiple pages in a DIMM module to be open at the same time, which increases the effective memory bandwidth by eliminating some RAS cycles.

SDRAM at 100 MHz

When using SDRAM on a 100-MHz memory bus, some special considerations and analysis are required. This section describes the 100-MHz SDRAM implementation method for the AMD-751 and the timing analysis required for reliable system design. An unbuffered SDRAM DIMM organization is used for this analysis.

For the 100-MHz SDRAM system, it is assumed that a maximum of 10 clock loads are allowed on one DIMM slot (single or double rows). This constraint implies the following:

- To support 4-bit wide devices, the zero delay buffer (ZDB) provides up to four clocks per DIMM to distribute the load.
- 8-bit wide devices can be used in single-row, unbuffered DIMM modules. Unbuffered DIMMs cannot be used in the case of dual-row DIMMs because of 16/18 loads on SRAS#, SCAS#, and MA[11:0].
- 16-bit wide and 32-bit wide devices have no restrictions.

Table 12 gives a more detailed SDRAM DIMM loading analysis.

Table 12. SDRAM DIMM Loading Analysis

DIMM Size	DIMM Organization	SDRAM Technology	Number of Rows/ Number of IC	Number of Loads MA/Ctrl[1]	Number of Loads SRAS#/CS#[2]	Number of Loads DQM	Number of Loads MD	Number of Load Clock
Unbuffered DIMM Modules								
8 Mbytes	1 Mbyte x 64	1 Mbit x16/16 Mbit	1/4	4	4	1	1	4
8 Mbytes	1 Mbyte x 72	1 Mbit x16/16 Mbit	1/6[3]	5	5	1	1	5
16 Mbytes	2 Mbytes x 64	1 Mbit x16/16 Mbit	2/8	8	4	1	2	8
16 Mbytes	2 Mbytes x 72	1 Mbit x16/16 Mbit	2/10[4]	10	5	1	2	10
16 Mbytes	2 Mbytes x 72	2 Mbit x 8/16 Mbit	1/9	9	9	1	1	9
32 Mbytes	4 Mbytes x 64	4 Mbit x16/64 Mbit	1/4	4	4	1	1	4
32 Mbytes	4 Mbytes x 72	4 Mbit x16/64 Mbit	1/6[3]	6	6	1	1	6
64 Mbytes	8 Mbytes x 72	8 Mbit x 8/64 Mbit	1/9	9	9	1	1	9
64 Mbytes	8 Mbytes x 64	4 Mbit x16/64 Mbit	2/8	8	4	1	2	8
64 Mbytes	8 Mbytes x 72	4 Mbit x16/64 Mbit	2/10[4]	10	5	1	2	10
Unbuffered DIMM Modules (difficult to support)								
32 Mbytes	4 Mbytes x 64	2 Mbit x 8/16 Mbit	2/16	16	8	1	2	16
32 Mbytes	4 Mbytes x 72	2 Mbit x 8/16 Mbit	2/18	18	9	1	2	18

Notes:

1. *Control includes SRAS#, SCAS#, or SWE#.*
2. *Row Chip Select.*
3. *In the JEDEC specification, 72-bit wide ECC DIMMs use two extra 4-bit wide devices for a single-row DIMM.*
4. *72-bit wide ECC DIMMS use four extra 4-bit wide devices for dual-row DIMMs. However, to reduce loading, two 8-bit wide devices are recommended.*

The SDRAM 100-MHz Scheme

To achieve the 100-MHz timing, a careful system timing analysis is required. Figure 16 shows the AMD-751 system controller clocking scheme.

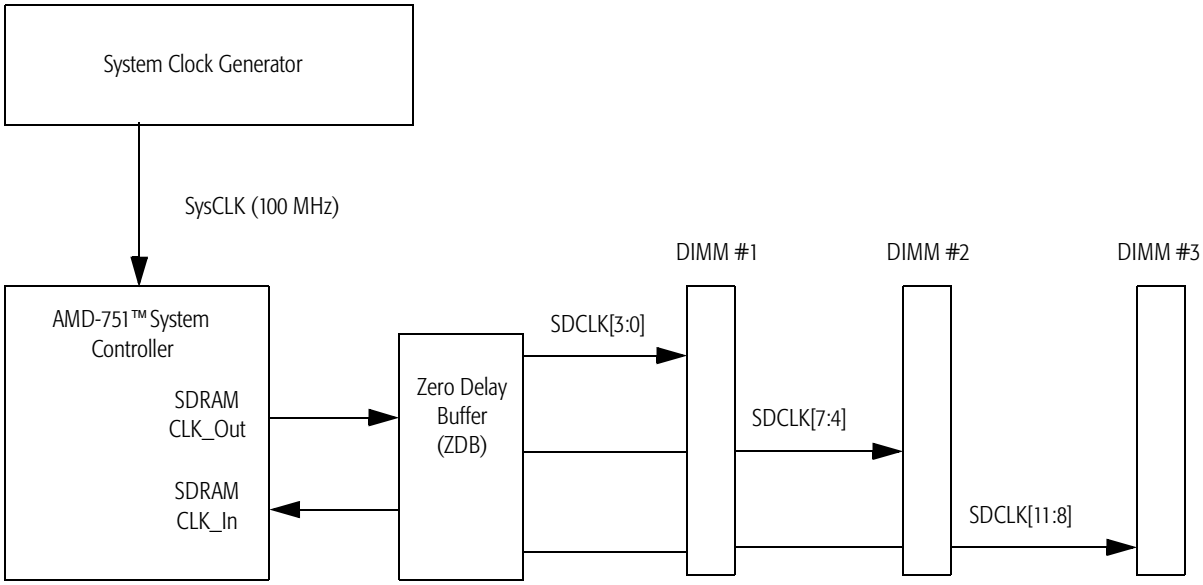


Figure 16. AMD-751™ System Controller Clocking Scheme

Delay Analysis

The most important two numbers in the clocking scheme are as follows:

- How early can the command (SRAS#, SCAS#), memory address (MA), and memory data (MD) be driven (in a write cycle)?
- How late can the returned data be latched?

Figure 17 on page 76 shows the 100-MHz SDRAM timing in detail. Table 13 on page 77 contains descriptions of the timing variables.

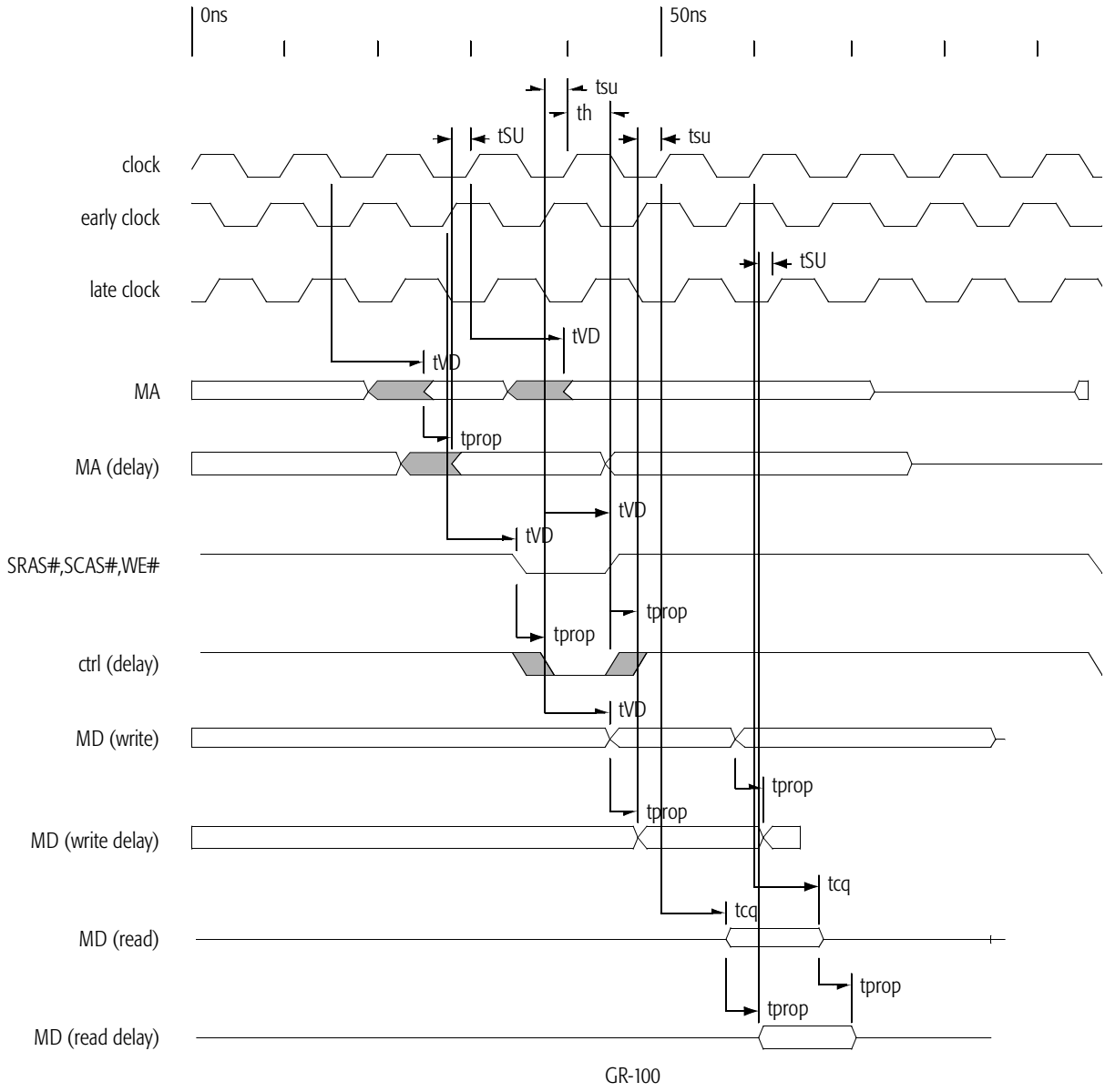


Figure 17. 100-MHz SDRAM Detailed Timing

Table 13. Key SDRAM DIMM Timing Variables

Timing Variable	SCAS#=3	SCAS#=2	Description
Tcl = Taa	3	2	SCAS# latency—The fundamental timing number that communicates how many cycles it takes to activate or read data. Tcl=4 is supported for buffered SDRAM.
Trcd	3–2	2	SRAS# to SCAS# latency—The delay from activation to RD/WR command.
Trc	8–7	5–7	Bank cycle time—The minimum time from activation to activation of the same bank, or auto refresh to activation (mode register set command).
Tras	5	3–5	Minimum bank active time—The time from activation to precharge of the same bank.
Trp	3	2	Precharge time—The time from the precharge command to when the bank can be activated again (mode register set or refresh).
Trw	1	1	Timing variable—Dictates R->W for how many NOP cycles must exist between RD and WR and when the data bus needs to be tri-stated before the last read data. Not configurable.
Tdimm	1	1	One cycle for DIMM turn-around time for page miss. Not configurable.
Trrd	2	2	Bank to different bank in same slot delay time—The delay from activating two banks within the same slot. Not configurable.

Signal Timing Analysis. The following equation calculates how early the AMD-751 system controller needs to send out SDRAM address and control signals. The calculation is as follows, with the reference as the external system clock:

$$t_{prop} = t_{cycle} - (t_{VD} + t_{ckskew} + t_{setup})$$

Where:

- t_{cycle}—100-MHz cycle time = 10 ns
- t_{VD}—Clock to output valid delay = 6 ns
- t_{ckskew}—Total allowable clock skew and phase error between the AMD-751 and SDRAM = 0.325 ns
- t_{setup}—SDRAM setup requirement = 2 ns
- t_{prop}—AMD-751 to SDRAM propagation delay < 1.675 ns

The result shows that, if the system clock is used to drive the SDRAM clocks, only a very short propagation delay is allowed. To allow greater propagation delays and compensate for the t_{VD} time, use a ZDB to drive the SDRAM clock.

For more information on SDRAM timing analysis, see the AMD-751™ System Controller SDRAM Cookbook, order# 22912.

5.4 PCI Bus Controller

The AMD-751 system controller drives the 32-bit PCI bus synchronously with the PCI clock (PCLK) supplied by the system clock generator. The AMD-751 converts the 64-bit processor data to 32-bit PCI data and regenerates commands with minimal overhead. A processor-to-PCI post write buffer enables the processor and PCI to operate concurrently. The AMD-751 converts consecutive processor addresses to burst PCI cycles. A PCI-to-DRAM post write buffer and a DRAM-to-PCI prefetch buffer enable concurrent PCI bus and processor-DRAM accesses during PCI-initiator transactions.

When the processor drives an I/O cycle to an address other than the AMD-751 system controller configuration register addresses, the AMD-751 passes the I/O cycle to the PCI bus. The AMD-751 posts the I/O cycle in one of its write buffers. The AMD-751 does not respond to I/O cycles driven by PCI initiators on the PCI bus. The AMD-751 allows these cycles to complete on the PCI bus. A memory write is the only transaction permitted from PCI to AGP.

Each PCI block can be broken up into two sub-blocks—the PCI target module and the PCI master module. The PCI target module handles cycles initiated by an external master on the PCI bus. The AMD-751 responds to cycles that are directed to main memory or writes that are sent to the other PCI interface. This module contains write buffers (PCI-to-memory and PCI-to-PCI), read buffers from memory, and a target sequencer that keeps track of the bus while the AMD-751 is a PCI target. Memory requests from both the PCI interfaces are sent through the MRO. See “AGP System DRAM Interface (SDI)” on page 90 for more information.

The PCI master module handles processor-to-PCI bus cycles. Within a processor stream, no reordering is done.

5.4.1 Memory Coherency

The AMD-751 system controller determines whether the data accessed through the PCI buses are coherent. Data written by the processor is made available for PCI reads and data from PCI writes is provided to the processor when it reads the same

location. If the PCI cycles get mapped through the GART, the AMD-751 performs one of the following actions to guarantee coherency:

- If this memory is cacheable, the processor should only access this memory through its physical address space and not through the GART. The PCI bus can access the memory either through the GART table address space or through the standard physical address space.
- If the processor cannot guarantee accesses to this space through the physical address space, it needs to use the same data type as in AGP (write-combining and noncacheable).

Note: *For more information about the GART, see "GART Cache Operation" on page 98.*

5.4.2 PCI Arbitration

The AMD-751 system controller contains arbitration logic that allocates ownership of the PCI bus among itself, the AMD-756 peripheral bus controller, and five other PCI initiators.

When there are no requests for the bus, ownership defaults to the processor through the AMD-751. *Parking* the bus in this manner is sometimes referred to as processor-centric arbitration. The AMD-751 can be programmed to be memory-centric, which parks the bus on the PCI master. This mode is controlled by device 0, offset 84h, bit 0 (see page 154).

5.4.3 PCI Configuration

The AMD-751 uses PCI configuration mechanism #1 to select all of the options available for interaction with the processor, DRAM, and the PCI bus. This mechanism is defined in the *PCI Local Bus Specification Revision 2.2*. All configuration functions for the AMD-751 are performed by using two I/O-mapped configuration registers—IO_CNTRL (I/O address 0CF8h) and IO_DATA (I/O address 0CFCh).

These two registers are used to access all the other internal configuration registers of the AMD-751. The AMD-751 decodes accesses to these two I/O addresses and handles them internally. A read to a nonexistent configuration register returns a value of FFh. Accesses to all other I/O addresses are forwarded to the PCI bus as regular I/O cycles. Read and write cycles involving the AMD-751 configuration registers are only distinguished by the address and command that is sent.

5.4.4 PCI Southbridge Signals

The AMD-751 supports one pair of PCI request/grant signals, PREQ# and PGNT#, to connect to a Southbridge device such as an ISA/EISA bridge. These signals are generally used when a PCI device, an ISA master, or a DMA device requires ownership of the system main memory. The ISA bus device asserts PREQ# to request the bus. The AMD-751 system controller grants the request after all of its write buffers have been flushed by asserting PGNT#.

Note: *The AMD-751 system controller allows a Southbridge device to hold PREQ# for an extended time in order to complete an ISA transfer and avoid a potential deadlock condition.*

5.4.5 PCI Parity/ECC Errors

The AMD-751 system controller indicates that an ECC error occurred on the memory bus by setting bit 15 in the status register (device 0, offset 07h–06h).

On the PCI Bus

The AMD-751 does not check parity on the PCI bus. The status bit (device 0, offset 07h–06h, bit 8) is always zero.

5.4.6 PCI-to-Memory/PCI-from-Memory and Other PCI Targets

The PCI target memory write FIFO is used to gather PCI writes-to-memory into cache lines. Only writes from a single PCI write transaction are gathered. By gathering them into complete cache lines, the probe (snoop) to the processor can invalidate the cache line instead of writing it back to the memory. In the case of a partial cache line write, the data is always written back to memory.

A dedicated PCI FIFO is used for writes going to the other A-PCI interface. In addition, this FIFO allows the PCI master to burst, gathering 32 bytes at a time, which improves performance.

The PCI target read FIFO is used to hold the cache line being read from memory. In addition, it is used to merge writeback data from the processor cache. The size of this FIFO is large enough to allow read prefetching.

5.4.7 PCI-to-Processor Bus Read Transactions

The AMD-751 contains an 8-byte read buffer that assembles two 32-bit PCI read cycles into one 64-bit quadword for the processor data bus. In addition, the buffers are used when any read crosses a 32-bit boundary. Aligned byte/word/doubleword processor reads are passed on to the PCI bus by the AMD-751 system controller. The read buffer is always enabled.

When the processor reads from the PCI bus, the AMD-751 acts as a PCI initiator. The AMD-751 responds to the read with data from one of its internal buffers, or with data obtained by performing a read operation on the PCI bus.

5.4.8 Processor-to-PCI Bus Write Transactions

The AMD-751 system controller converts a full 64-bit (quadword) processor-to-PCI write into two consecutive 32-bit (doubleword) PCI write cycles. This feature reduces the bus bandwidth required to complete PCI writes.

The AMD-751 contains a post-write buffer between the processor and the PCI bus. Every processor-to-PCI write is stored in the buffer unless it is full, allowing the processor to begin its next operation without having to wait for the write to complete. When the PCI bus is available, the AMD-751 performs up to five 32-bit PCI writes to complete the transaction.

Processor To/From the PCI Buses (PCI Master)

The PCI master write FIFO is used to store the data for a processor-to-PCI write, which allows concurrent writes to both PCI buses. The architecture support is optimized for 64-byte transfers. In addition, this FIFO can hold multiple smaller transfers. In the case of video capture cards sitting on the standard PCI bus, PCI-to-AGP PCI write cycles are also sent through this buffer.

The PCI master read FIFO is able to hold the largest processor read from the secondary PCI bus. The standard PCI bus is optimized for single quadword accesses.

Burst Cycles

The AMD-751 writes all of its buffer contents in a single PCI transaction when the bus becomes available. In this way, consecutive processor-to-PCI writes, whether two full quadwords or several smaller transactions combined through byte merging, are performed in a single PCI transaction.

5.4.9 PCI Accesses by An Initiator

A PCI initiator begins a memory read or write cycle by asserting FRAME# and placing the memory address on AD[31:0]. The AMD-751 system controller decodes the address. If the address is within the domain of the processor or memory, the AMD-751 accepts the cycle and responds as a PCI target by asserting DEVSEL#. If the address is not within the AMD-751 or processor domain, the AMD-751 ignores the cycle and allows it to complete on the PCI.

Prefetch Options

Read requests from the PCI block to the MRO are made in terms of cache lines only. After fetching the initial cache line, it is possible to start prefetching the next cache line. Prefetching the next cache line is preferred, because the PCI master typically reads more than one line, but can waste DRAM bandwidth if this line is thrown away.

Read/Write Request

The length of a read request is always eight quadwords (one cache line). During writes, the AMD-751 attempts to accumulate an entire cache line. If the start address is not cache aligned, the AMD-751 makes single write requests until it gets cache aligned. When aligned, it makes a request every eight quadwords. Each time a write request is made, the request length is reset. If a partial quadword write is detected, no more data is accumulated and a request is issued. When there are a few accumulated quadwords and then there is a partial quadword write, the request is broken up into two requests—one request with the current length minus 1 containing all enabled bytes, and one request of a single partial-quadword write. This splitting up of requests is done in the PCI SDI request queue.

Request Queue

When the queue is empty, the request passes through and is sent directly to the SDI and the other PCI bus. If the SDI is not ready to accept the request or there is a GART translation involved, the request is held in the queue.

Write Data and Byte Enables

The PCI data bus is 32 bits wide while main memory and internal data buses within the AMD-751 are 64 bits wide. When a PCI write occurs to memory (and the other PCI interface), two consecutive doublewords are accumulated into a quadword of data. In addition, the corresponding byte enables are accumulated. Data and byte enables corresponding to the lower doubleword are latched. When the high doubleword is written, this data along with the latched lower doubleword are written to the write data FIFO. When there is no write to the upper doubleword, the corresponding byte enables must be inactive while writing the latched lower doubleword to the write data FIFO. If the first write is to the upper doubleword, the lower byte enables must be masked off.

5.5 Accelerated Graphics Port (AGP)

The accelerated graphics port (AGP) is a point-to-point connection between a graphics adapter (AGP initiator) and a memory controller (AGP target) that enables the adapter to store and use graphics data in main memory. This connection relieves graphics traffic from the PCI bus and greatly accelerates video performance.

The AMD-751 system controller functions as an AGP target, providing all the signals, buffers, and logic required for full compliance with AGP specification version 1.0.

AGP Features

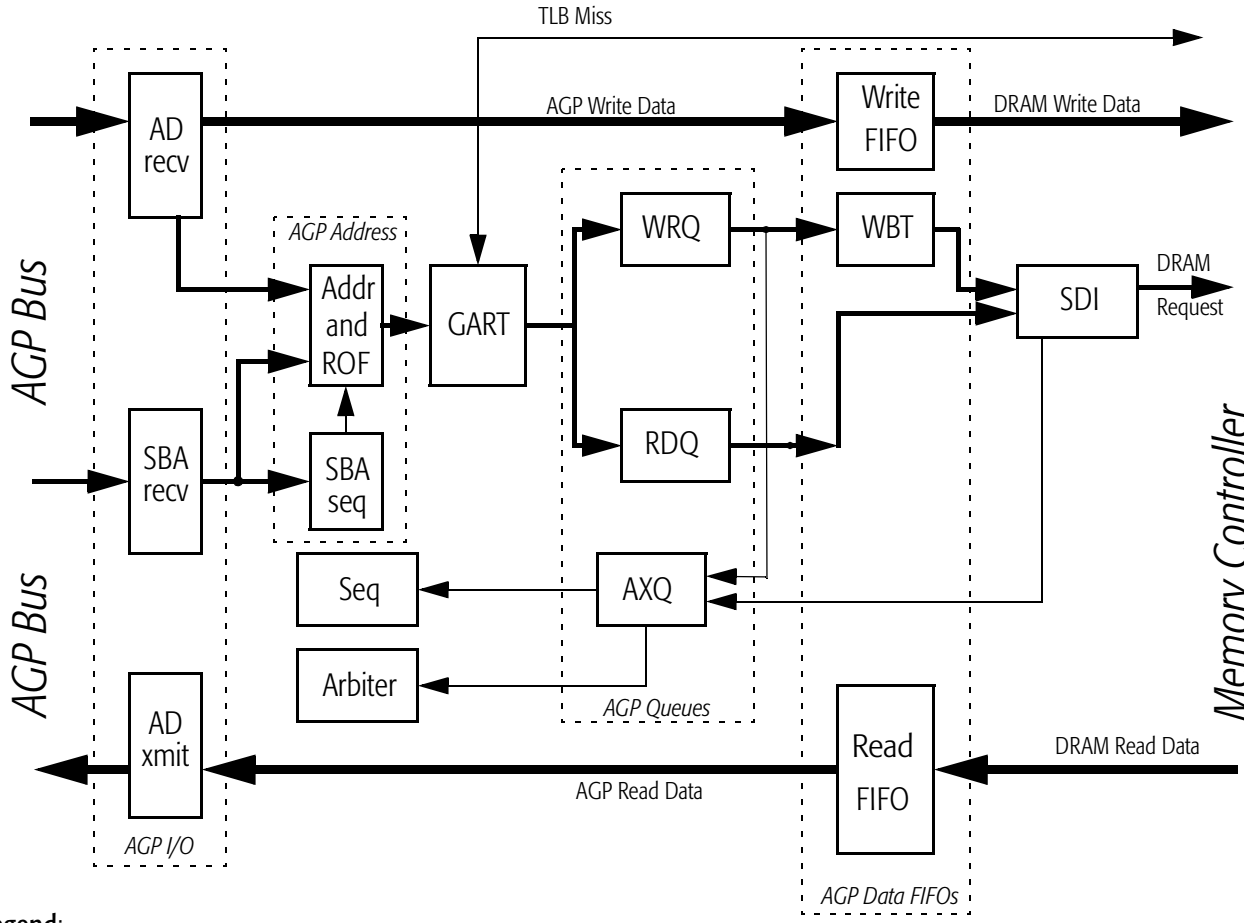
While AGP relieves traffic on the PCI bus and frees up graphics adapter memory, the greatest impact on system performance comes from the many innovations AGP brings to data transfer operations. These improvements include the following:

- *Split Transactions*—Requests to read or write data are separate from the data transfers.
- *Pipelined Requests*—Requests can be issued contiguously and stored in the AMD-751 system controller request queue. Pipelining allows AGP to achieve high levels of concurrency with PCI and the processor.
- *Pipeline Grants*—Pipelined GNT# signals for up to four write transactions.

- *Prioritizing* (reordering)—Read and write requests can be assigned a high priority or a low priority to ensure that more urgent requests are serviced first.
- A command set geared toward optimizing queued, prioritized requests.
- *Defined-Length Requests*—The amount of data requested is indicated in the AGP command, rather than the duration of an asserted signal, such as FRAME# in PCI.
- An 8-byte minimum data size for AGP 2x transfers, which provides a more efficient method for moving the large amount of data typical in a graphics request.
- A separate, optional sideband address (SBA) bus that enables concurrent transmissions of requests and data transfers.
- An optional 2x mode that doubles the AGP graphics adapter data transfer rate (double-pumped transfers at 66 MHz).
- Freedom from the coherency requirements of PCI, which eliminates the latency resulting from cache snooping.
- Full PCI 2.2 capability, which enables the AMD-751 to pass programming information from the processor to the graphics adapter.
- A deep request queue.
- A graphics address remapping table (GART). See "GART Cache Operation" on page 98 for more information.

5.5.1 AGP Block Diagram

Figure 18 shows the AGP block diagram.



Legend:

AD xmit	AD Bus Transmitter	SBA	Sideband Address
AXQ	AGP Transaction Queue	SDI	System DRAM Interface
RDQ	Read Request Queue	seq	Sequencer
recv	Receive	WBT	Write Buffer Tag
ROF	Reorder FIFO	WRQ	Write Request Queue

Figure 18. AGP Block Diagram

GART Cache

The GART cache is made up of the GART directory caches (GDC) and the GART table cache (GTC). The request is read out of the queue in the address module, and the virtual address is translated into a physical address. If the corresponding GART entry is not present, a request is sent to the ATE, a GART table walk is performed, and the entry is fetched from the memory.

See "GART Address Translation Engine (ATE)" on page 100 for more information.

5.5.2 The AGP Queues

This section describes the queuing structures in the AMD-751 system controller AGP block. There are two types of queues—request queues and transaction queue.

When an AGP request is detected, either in the standard PIPE# mode or through the SBA mode, it is written to the request queues. These queues sort the request based on priority and present the next request to be serviced (based on priority). There are two queues—one for reads and one for writes, each with a depth of eight entries. Because the output of these two request queues goes to different blocks, they can both send out requests at the same time.

The AMD-751 queues and data buffers streamline AGP read and write requests and data transfers. These queues and buffers are shown in Figure 19 on page 87.

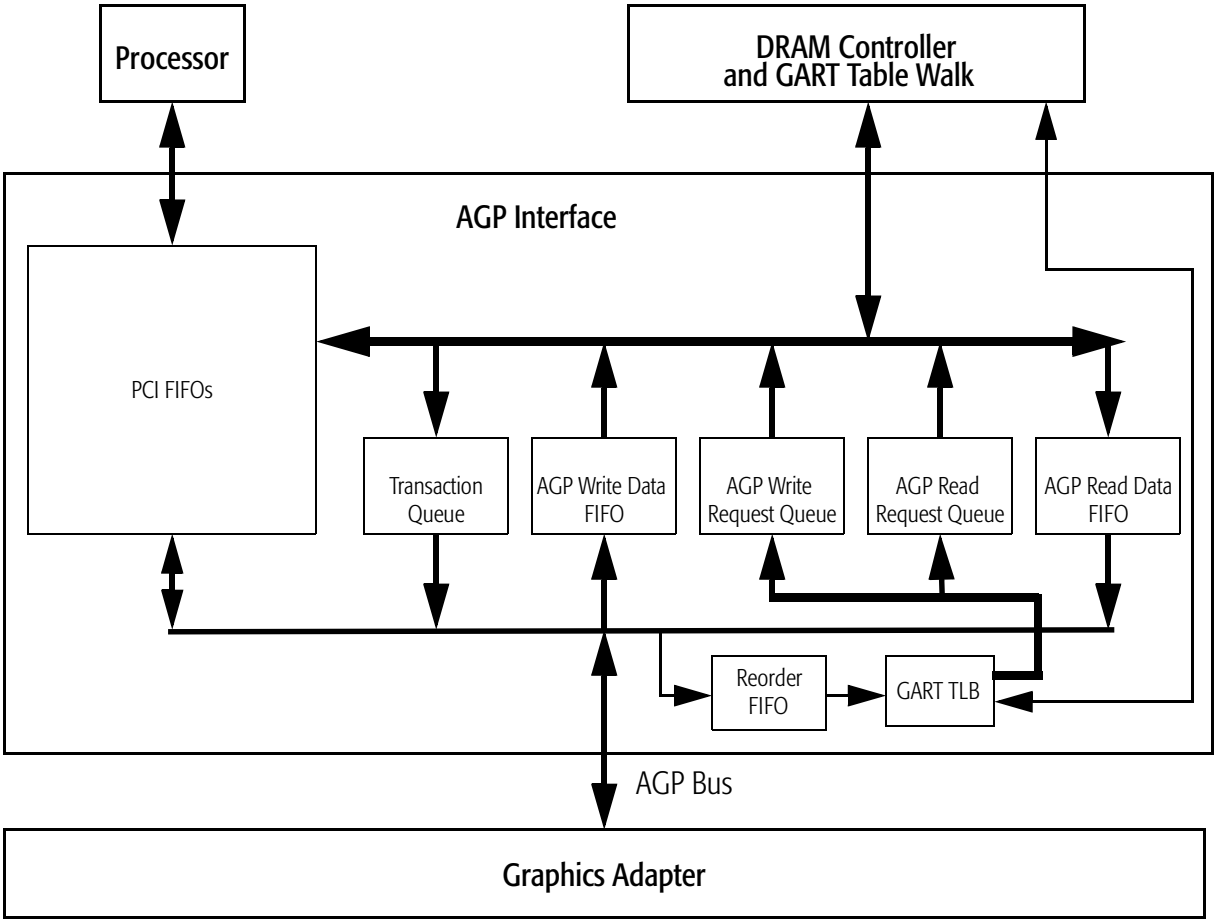


Figure 19. AGP Queues and Buffers

AGP Request Queue

The AGP request queue has the following specifications:

- Two queues—one for read requests and one for write requests.
- 40 bits per entry in each of the request queues.
- Holds the GART-translated physical address.
- Each queue automatically reorders high-priority requests in front of low-priority requests.
- The write request queue (WRQ) interfaces to the write buffer tag (WBT) and the AGP transaction queue (AXQ).
- The read request queue (RDQ) interfaces to the SDI and the read acknowledge queue (RXA).
- Requests can be issued from both the write queue and read queue in the same clock.

Structure of the AGP Request Queue

The AGP request queue is split up into two queues—one for read requests and one for write requests. Because there is a reordering FIFO in the address module, the request queues do not have to be large. The read queue is big enough to hold all outstanding read requests, which avoids stalling writes that run on the bus while the reads are being done on memory.

Requests from the SBA bus are multiplexed with PIPE# requests and written to the same queues. High-priority requests are inserted in front of low-priority requests so that the request to be serviced is at the top of the queue. This reordering is done dynamically as a new request is written into the queue.

Because requests from each of the queues go to a different sub-block, requests can be read out of both the queues at the same time. The DRAM starts fetching data from memory and the write data is sent across the AGP bus at the same time.

Read Ordering with Respect to Writes

The AGP ordering rules specify that writes are ordered ahead of reads. Reads are serviced only when all the preceding writes have been written to memory, which is only required for low-priority requests and does not affect high-priority read requests. When a low-priority request is the next one to be serviced from the read queue, the tag of that request is sent to the write queue module and WBT modules. The tag is compared with all valid entries in the two modules. If any of them hits (matches), the read request is blocked. After the write requests get serviced, the read is allowed to proceed.

AGP Request Queue. In general, the AGP request queue services AGP requests in the order received, subject to their priority (read high, write high, read, write).

Ordering Rules. The request queue is subject to the following AGP ordering rules:

- Read requests are processed in the order they are received.
- Write requests are processed in the order they are received.
- Reads push writes, meaning that a write request is serviced before a subsequently received read request is serviced.
- Writes can pass reads, meaning that a write request can be serviced before a previously received read request.
- There are no ordering restrictions between AGP and PCI transactions on the AGP bus.

- PCI transactions on the AGP bus follow the PCI ordering rules described in the PCI Local Bus Specification, Revision 2.2.
- High-priority reads and writes bypass low-priority reads and writes.

If a low-priority data transfer is in progress when a high-priority request is received, the data transfer completes before the high-priority request is serviced—that is, a request is not preemptable. A high-priority request supersedes a low-priority request on a request boundary only.

The AMD-751 system controller ignores the processor LOCK# signal when the graphics adapter reads a location in memory that is currently locked by the processor. In addition, the AGP PCI bus does not honor LOCK# from the primary PCI bus. If a PCI master attempts to access a locked location, the access proceeds normally and generates a retry (or an SERR#). Using LOCK# can result in a system hang or other operational problems. LOCK# is not normally used on the PCI bus and its use should be avoided. In addition, because AGP does not enforce coherency, read requests can return stale data and write requests can be overwritten by cached data when it is written back.

AGP provides two commands, Flush and Fence, to give software control over request ordering.

Fence Command

The Fence command ensures that all requests preceding it are processed before all requests that follow it. Write requests issued after the Fence command do not pass read requests issued before the Fence command.

Flush Command

The Flush command forces the immediate servicing of all write requests in the request queue. A single quadword of random data is returned when the last write is completed. This process forces all data residing in the AMD-751 system controller buffers to be visible to the rest of the system, ensuring that a subsequent memory access returns the correct AGP data.

After the flush request gets queued, and until it is serviced, any high-priority write requests entering the queue are serviced before the flush occurs.

AGP Transaction Queue

The AGP transaction queue (responses to AGP requests) holds information about transactions that are ready to run on the AGP bus. Write transactions are put into this queue as soon as the request is retired from the request queue. Read transactions only enter this queue after some data for that transaction is available in the read buffer. The arbiter looks at this queue to decide which transaction should be granted the bus next. In addition, the bus sequencer looks at this queue to know what transaction to run next. The order in which the transactions are sent to the queue is the order in which the transactions are run on the bus.

5.5.3 AGP System DRAM Interface (SDI)

The AGP logic interfaces with the MCT through the system DRAM interface (SDI). The SDI gets write requests from the write buffer and read requests from the read request queue. It arbitrates between these two requests and sends the request on to the MCT. In addition, it is responsible for breaking requests down to the size that the MCT can accept and making sure that requests do not cross a DRAM page boundary. The SDI has a two-level pipeline so that, if there are a number of small requests pending, it can continuously accept these requests and send them on to the MCT on every clock.

Memory Request Address and Length Calculation

In an x86 system, the memory burst sequence is interleaved and the AGP burst sequence is linear. Therefore, bursts can be done only when they are aligned to a cache-line boundary. The maximum size of a request to the memory controller is eight quadwords. The SDI sub-block checks that the address is cache-line (or four quadword) aligned. If it is not aligned, the AMD-751 system controller requests single quadwords. Otherwise, the AMD-751 requests an entire block (eight quadwords). In addition, in the case of writes, if all the bytes in the transaction are not enabled and if ECC is enabled, the transaction is broken down into single quadword transfers.

5.5.4 AGP Arbitration

The AGP arbiter is responsible for granting the bus to the master in response to a bus request, and for scheduling data transactions that are ready to run on the AGP bus. In addition, the AGP arbiter can generate pipelined data grants to get the maximum bandwidth.

There are three different arbiters in the AMD-751 system controller—the PCI arbiter, the memory arbiter, and the AGP arbiter. The relationship between these three arbiters and their various inputs is shown in Figure 20.

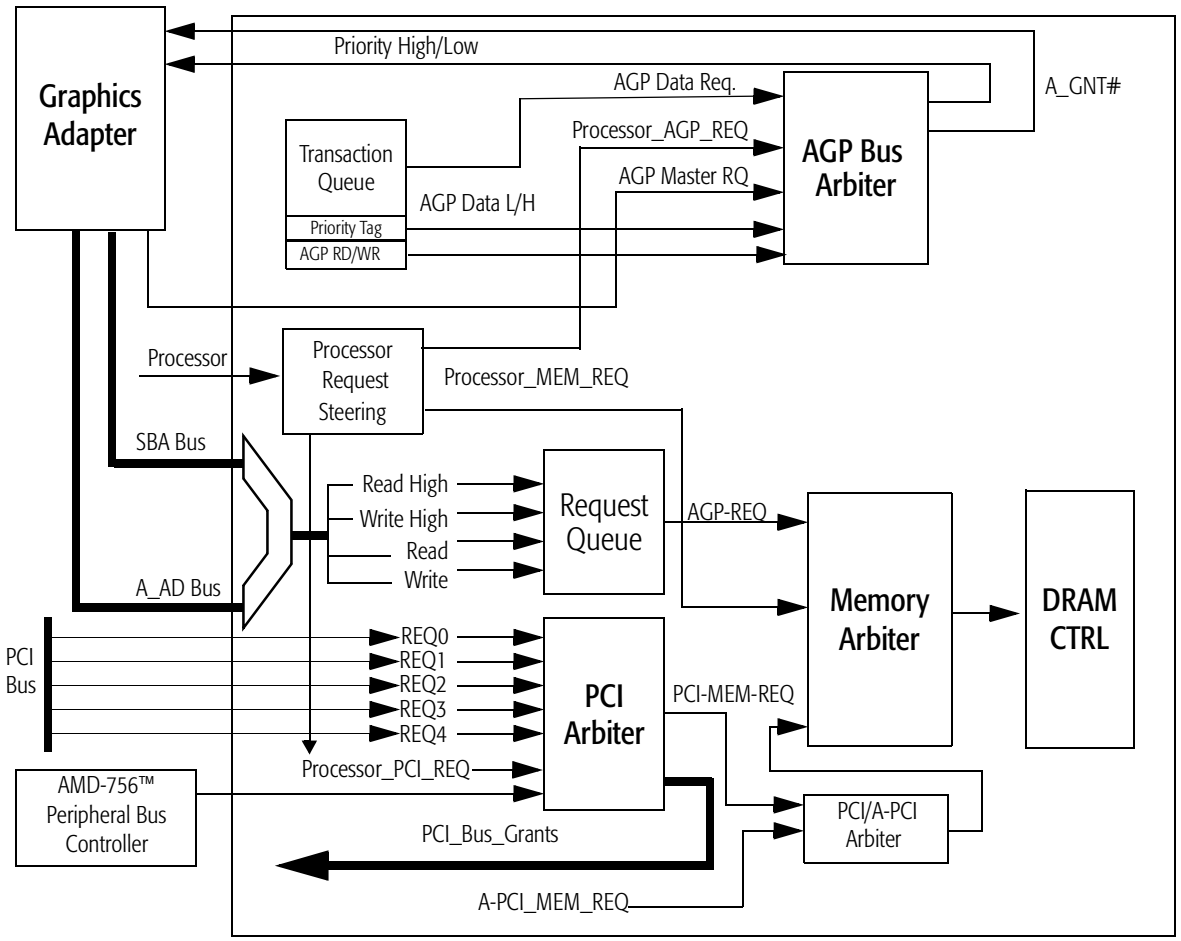


Figure 20. AMD-751™ System Controller Arbiters

PCI Arbiter

The PCI arbiter receives requests from the processor, the AMD-756 peripheral bus controller, and other PCI agents, and determines which request is serviced on the PCI bus.

Memory Arbiter

The memory arbiter receives requests from the processor, the PCI arbiter, and the AGP request queue. Requests are serviced on a first-come, first-serve basis.

AGP Bus Arbiter

The AGP bus arbiter prioritizes requests for the AGP bus in the following order:

1. High-priority data
2. AGP accesses from the processor
3. PCI requests from the graphics controller
4. Low-priority data

High-priority AGP requests are serviced before any other AGP bus requests. The processor is second in the priority chain, ensuring that it is not locked out by other requests. However, processor traffic to the frame buffer can constitute a significant portion of the traffic on the AGP bus. Back-to-back processor requests with a tight polling loop could starve out the ability of the graphics controller to queue new transactions and prevent the transfer of low-priority AGP data. To avoid this situation, systems employing polling loops rather than interrupts should pad the loops with delays.

Graphics controller (AGP master) address requests and PCI cycles are third on the AGP bus priority chain. These requests have priority over low-priority AGP data transfers, guaranteeing that the new transactions are queued using brief bus cycles by asserting PIPE#. This prioritization allows the request pipeline to stay full.

Low-priority AGP data transfers have the lowest AGP bus priority so that transactions, such as a series of long reads, do not starve processor accesses to the frame buffer or the AGP request pipeline.

5.5.5 AGP Data

The minimum granularity of AGP data transfers is eight bytes, and data is always aligned on 8-byte boundaries. Smaller transfers must be done through PCI cycles. AGP cycles incur substantially less processor overhead than PCI cycles because the caches are not snooped. However, data coherency is lost. Data transfers requiring coherency should be transferred with PCI cycles.

To service an AGP read request, the AMD-751 system controller reads the requested data from memory, stores it in its 64-quadword read data FIFO, and sends it to the adapter during AGP data phases. To service an AGP write request, the controller accepts data from the adapter during AGP data phases and stores it in its 16-quadword write data FIFO until it can write the data to memory.

5.5.6 PCI Transactions on the AGP Bus

Using the secondary PCI bus—that is, performing PCI transactions on the AGP bus—is preferable or necessary in some circumstances. To program control information into the graphics adapter, the AMD-751 system controller configures the PCI registers of the adapter through the secondary PCI bus. If the adapter must perform a memory read smaller than eight bytes (the minimum AGP data size), it can do so by using a PCI transaction. PCI transactions are required in cases where data coherency must be maintained, because AGP cycles do not generate cache snoops.

A secondary PCI transaction is indicated by the assertion of A_FRAME#. The AMD-751 system controller maintains a separate buffer for PCI transactions that use the AGP bus. The adapter can write to a PCI device but cannot read from one. The AMD-751 supports PCI-to-AGP writes and AGP-to-PCI writes but does not support AGP-to-PCI reads or PCI-to-AGP reads.

5.5.7 Graphics Adapters and Main Memory

To work with data stored in main memory, a graphics adapter must either load the data into its local memory or manipulate the data in place in main memory. The AGP specification refers to these two approaches as *DMA mode* and *execute mode*, respectively. While the AMD-751 system controller can implement either approach, the execute mode more effectively reduces the burden on graphics adapter memory, which is a primary objective of AGP.

5.5.8 AGP Virtual Address Space (Aperture) Range and Size

The GART aperture defines the amount of memory allocated to the AGP virtual address space. There are seven different AGP aperture sizes available—32 Mbyte, 64 Mbyte, 128 Mbyte, 256 Mbyte, 512 Mbyte, 1 Gbyte, and 2 Gbyte. Depending on the selected AGP aperture size, address bit 31 to bit nn (where nn is a variable bit number) of the issued AGP virtual address is used for a GART range check. Address bits nn–1 to 12 are used for translating the virtual address to a physical address.

A graphics adapter requires a contiguous view of memory, but most systems allocate memory in non-contiguous blocks. To accommodate this disparity, the AMD-751 system controller implements a graphics adapter remapping table (GART) described in the AGP Interface Specification, Revision 2.0. The GART translates the contiguous addresses used by the adapter (referred to as virtual addresses) to their actual, generally not contiguous, physical addresses in main memory. The GART acts much like the page table in the processor, mapping linear addresses to physical addresses. Figure 21 shows this remapping.

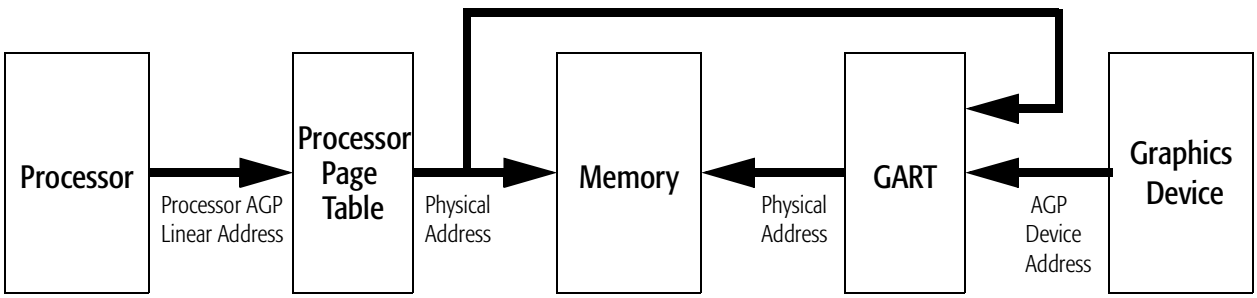


Figure 21. Address Remapping

The GART table or tables reside in memory. They are set up and maintained by device driver calls through application programming interface (API) routines as defined in the AGP specification. Each entry in the table(s) correlates a virtual address with a physical address. Configuration registers in the AMD-751 system controller determine the location of the table(s) in memory, and the location and size of the AGP memory block to which the GART translates its addresses.

Conventional (Two-Level) GART Scheme

The GART scheme is a conventional two-level scheme. The scheme is designed to accommodate the 4-Kbyte pages employed by many systems, and requires two memory accesses to translate the AGP virtual memory address to the actual physical memory address.

The size of a table is constrained to one page (4 Kbytes). Each entry address is four bytes, limiting the table to a maximum of 1-Kbyte entries. To enable the use of more than 1-Kbyte entries, the conventional scheme employs multiple 1-Kbyte-entry GART tables, each containing 1024 virtual address/physical address translations. Each GART table entry is four bytes in length. Bits 31–12 are the base address of a 4-Kbyte page in system memory. Bits 11–2 are reserved for future use. Bit 1 is always ignored, and bit 0 is the valid bit. The GART table base address is aligned on a 64-Kbyte boundary initialized by the device driver in the GART base address register.

The memory location of each GART table is tracked in a separate, 1-Kbyte-entry GART directory. Therefore, there can be up to 1024 GART tables. In addition, each GART directory entry is four bytes in length, with bits 31–12 containing the corresponding GART table base address. Bits 11–2 are reserved for future use, bit 1 is ignored, and bit 0 is the valid bit for the entry. The base addresses of the GART directory and GART tables are all 64-Kbyte aligned.

The AMD-751 system controller contains the following two on-board translation lookaside buffers (TLB), which reduce the number of memory accesses to the GART:

- An 8-entry fully associative GART directory cache (GDC).
- Three fully associative GART table caches (GTC).

Figure 22 and Figure 23 show the GDC and GTC hierarchy. See "GART Cache Operation" on page 98 for more information.

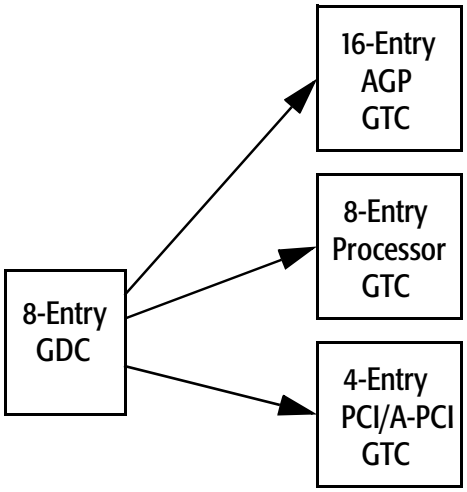


Figure 22. Cache Hierarchy (Conventional Two-Level Scheme)

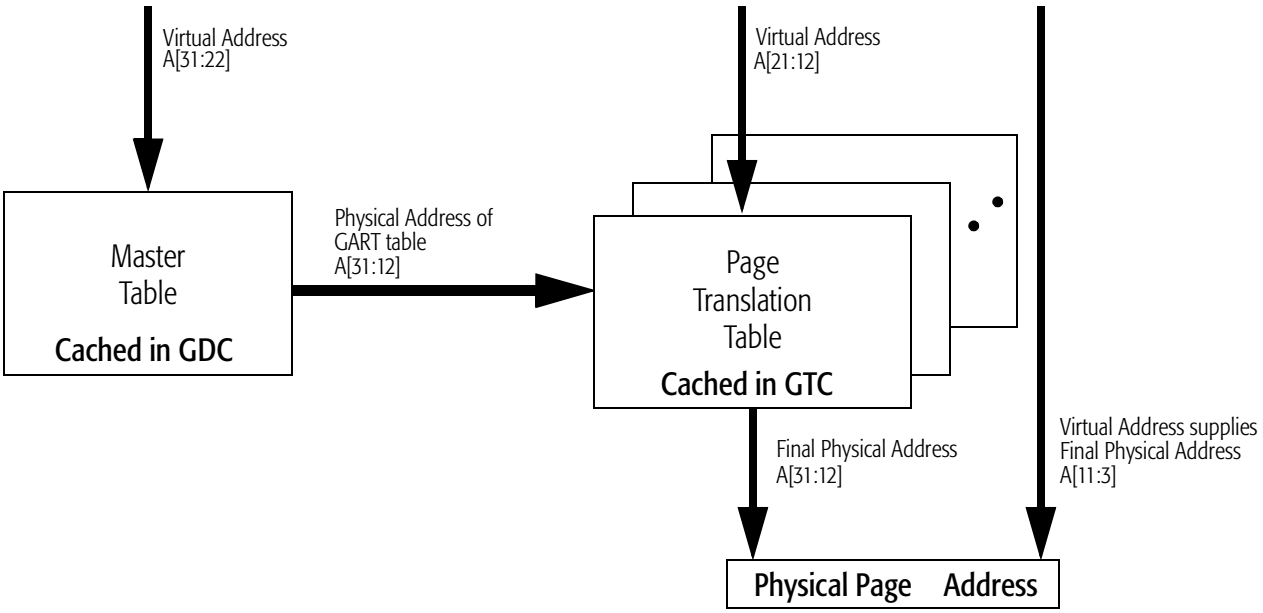


Figure 23. Conventional GART Scheme—Multiple Tables

When an address issued by the graphics controller (the virtual address) falls within AGP memory range and misses both of the GART caches, two memory accesses take place. The first access uses AGP virtual address A[31:22], concatenated with the page directory base, to select an entry from the GART directory. This entry contains the 20-bit base address A[31:12] of the GART page table to be used. The second memory access uses AGP virtual address A[21:12] to select an entry in the GART table. This entry contains the final physical page address (PPA). Figure 24 shows the two memory accesses.

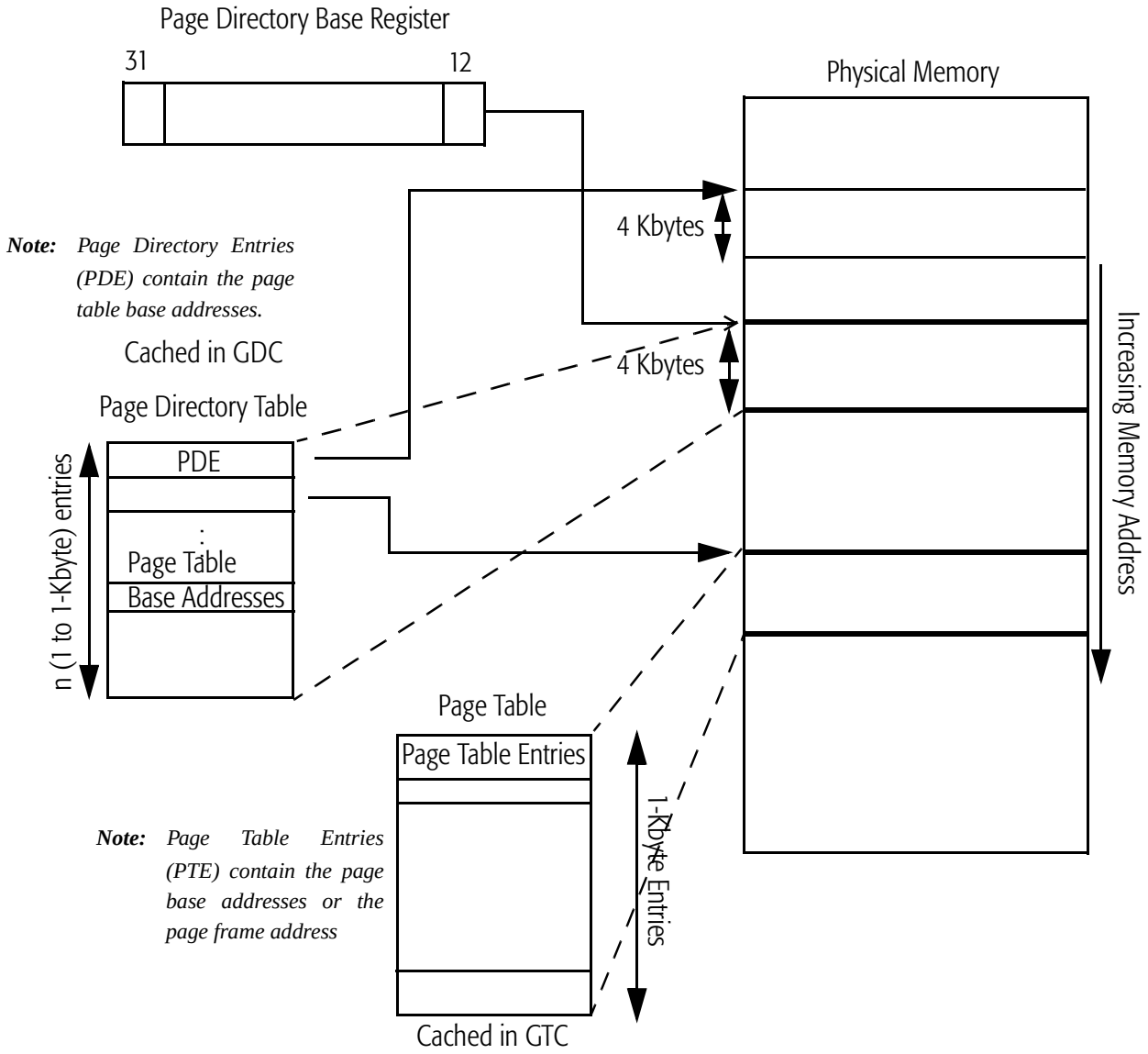


Figure 24. Page Translation Structures

GART Table Cache (GTC) The GART table cache (GTC) consists of the actual cache that stores the physical addresses corresponding to the most recently accessed virtual addresses and associated state machine. The GTCs are distributed amongst all the agents that require GART translation. Therefore, there are three GTCs in the AMD-751 system controller.

GART Table Walk The GART table walk (GTW) consists of the Table Walk state machine, a centralized resource that also contains the GART directory cache common to all GTCs. See "GART Address Translation Engine (ATE)" on page 100 for more information.

GTC Front End The GTC front end consists of agent-specific hooks required for optimizing normal operation (for example, AGP-required page crossover detection on accesses performed before the request enters the AGP request queue).

5.5.9 GART Cache Operation

Table 14 summarizes GART terminology used in this section.

Table 14. Summary of GART Terms

Term	Abbreviation	Location	Cached In:	Translation
Page Directory Table	PDT	Memory	GDC	1st level
Page Directory Entry	PDE	Memory/GDC	GDC	1st level
GART Directory Cache	GDC	AMD-751		1st level
GART Front End	GFE			
Page Tables	PT	Memory	GTC	2nd level
Page Tables Entry	PTE	Memory/GTC	GTC	2nd level
GART Table Cache	GTC	AMD-751		2nd level

The AMD-751 system controller contains three GART table caches (GTCs) and an 8-entry GDC. In the two-level scheme, a virtual address that hits the GTC cache can be translated to its physical address without any memory accesses. Missing the GTC, but hitting the GDC cache requires only one memory access. Missing both caches requires two memory accesses.

The GTC and GDC are hardware-driven and transparent to the system software except during initialization or modification by chipset device-driver management software. Configuration space register bits are used to enable, disable, flush, and purge

GTC and GDC entries. See device 0, offsets ACh–B3h and memory mapped registers at BAR1 + offset 00h to 13h. Figure 25 shows the structure of page table entries.

31. 12	11	10	9	8	7	6	5	4	3	2	1	0
Page Base Address	R	R	R	R	M2	M1	M0	R	R	R	R	P

Figure 25. Page Directory Entry (PDE) Definition

The bits in Figure 25 have the following definitions:

- Bit 0—Present bit
  - 1=Present and Valid
  - 0=Not Present/Page Not Valid
- Bits 4–1 Reserved for future use
- Bits 7–5 —TLB lookup mask bits M[2:0]. A 1 in any bit position masks that bit from being compared during lookup. See Table 15 for the proper use of the mask bits.

Table 15. Mask Bits

Number of Pages	M2	M1	M0
1	0	0	0
2	0	0	1
4	0	1	1
8	1	1	1

- Bits 11–8—Reserved for future use
- Bits 31–12—4-Kbyte Page Base Address

The page cacheable bit indicates the cacheability of the page in the processor caches. If the page is cacheable, any AGP/PCI access to a virtual address that translates to the physical address of this page, and whose PC bit is set, must snoop the processor cache with this physical address.

The PC bit is set in the page table/page directory entry in the GART by the miniport driver when 4-Kbyte pages are reserved by the graphics application.

For texture data, the page is usually uncacheable. For geometry data, it is advantageous for the page to be cacheable.

Distributed GART—GDC Features

The GART directory cache (GDC) contains three GART table caches (GTC)—one each for the processor, AGP, and PCI/A-PCI. These GTCs have the following features:

- The AGP GTC is a 16-entry, fully associative cache.
- The processor GTC is an 8-entry, fully associative cache.
- The GTC for PCI/A-PCI is a 4-entry, fully associative cache.

GART Table Cache (GTC)

The AGP GTC is a 16-entry, fully associative cache for storing the most recently used page address translation information. The implementation for the GTC returns a physical address for a GTC hit in one clock.

The GTCs are distributed TLBs. The entire TLB array is used for each agent that requires GART translation, which minimizes table walks for accesses from each agent. The GTC sizes in each agent are different.

GART Address Translation Engine (ATE)

The GART address translation engine (ATE) is a state machine responsible for the entire address remapping process, which includes the following functions:

- Routing the AGP virtual address to the GTC and/or GDC
- Conducting cache searches
- Initiating a memory request for a GART directory or GART table entry after a cache miss
- Deriving the physical address either from cache or memory
- Routing the physical address to the DRAM controller

GART Table Walk (GTW). The GART table walk is part of the ATE state machine that handles the table walk functions for GTC misses from each of the GTCs, and fetches the translated physical address top-of-page from the table entries in memory.

Figure 26 on page 101 shows the address translation flow.

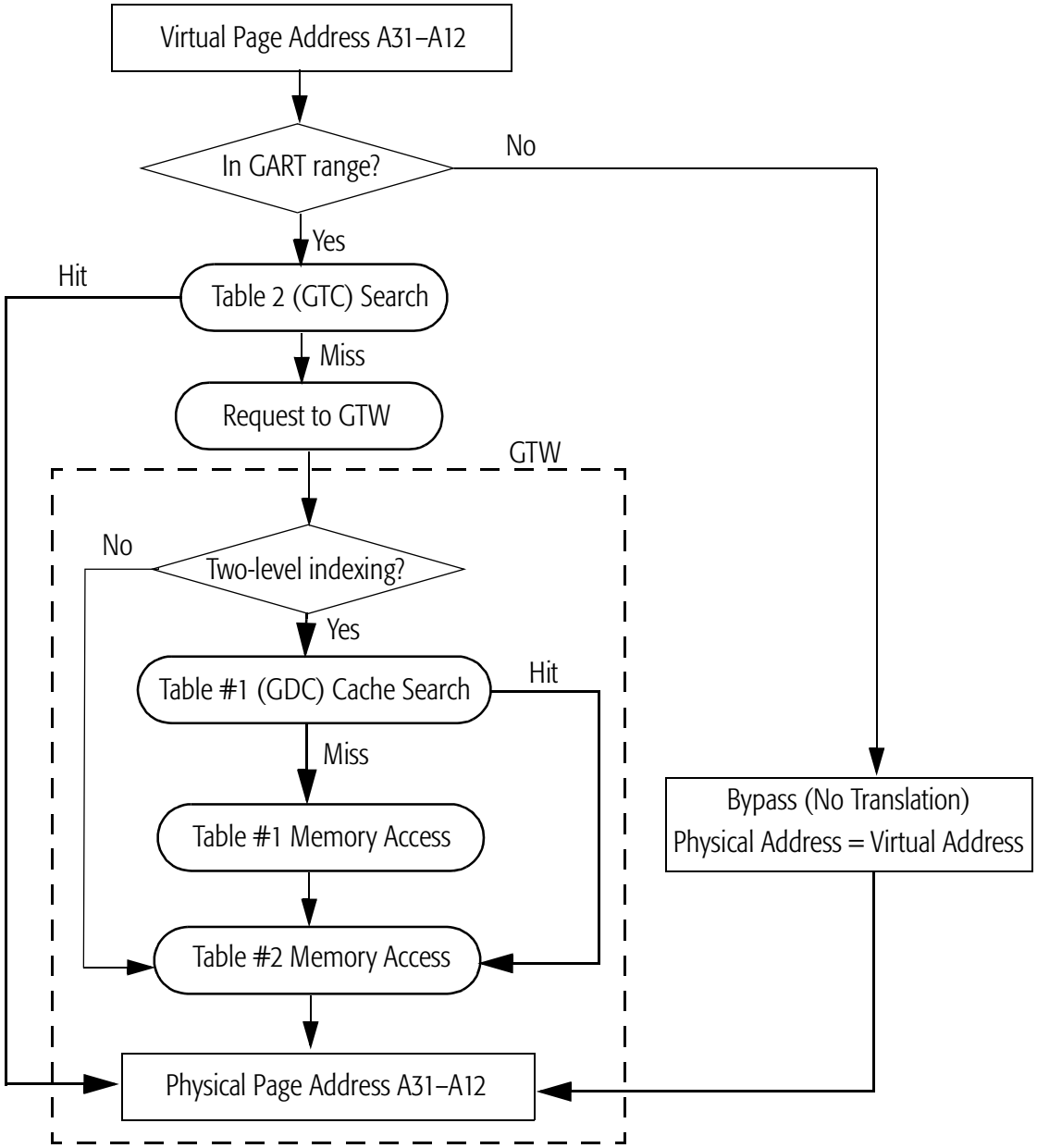


Figure 26. Address Translation Flow Chart

Page Directory Entry (PDE)

Each PDE is 32-bits wide. Bits 31–12 form bits PA[31:12] of the physical address (PA) used to fetch the PDE. Bits 11–2 are formed by bits 31–22 of the linear address provided by the graphics master. Bits 11–8 of the PDE are reserved for future use, bits 7–5 are mask bits (see Table 15 on page 99), and bits 4–1 are reserved. Bit 0 indicates a valid entry.

Bits 31–12 of the PDE concatenated with bits 21–12 of the linear address form the 32-bit page table address from which the page base address is fetched from memory.

Note: *Bits 21–12 of the linear address represents bits 11–2 of the page table address (or the page table offset).*

Bits 31–12 of the page base address, concatenated with bits 11–3 of the linear address (that is, the page offset) forms the physical address in memory from which the operand is finally fetched. Figure 27 on page 103 and Figure 28 on page 104 show this translation scheme.

The page directory table (PDT) contains up to 1-Kbyte entries, depending on the amount of remapped graphics memory.

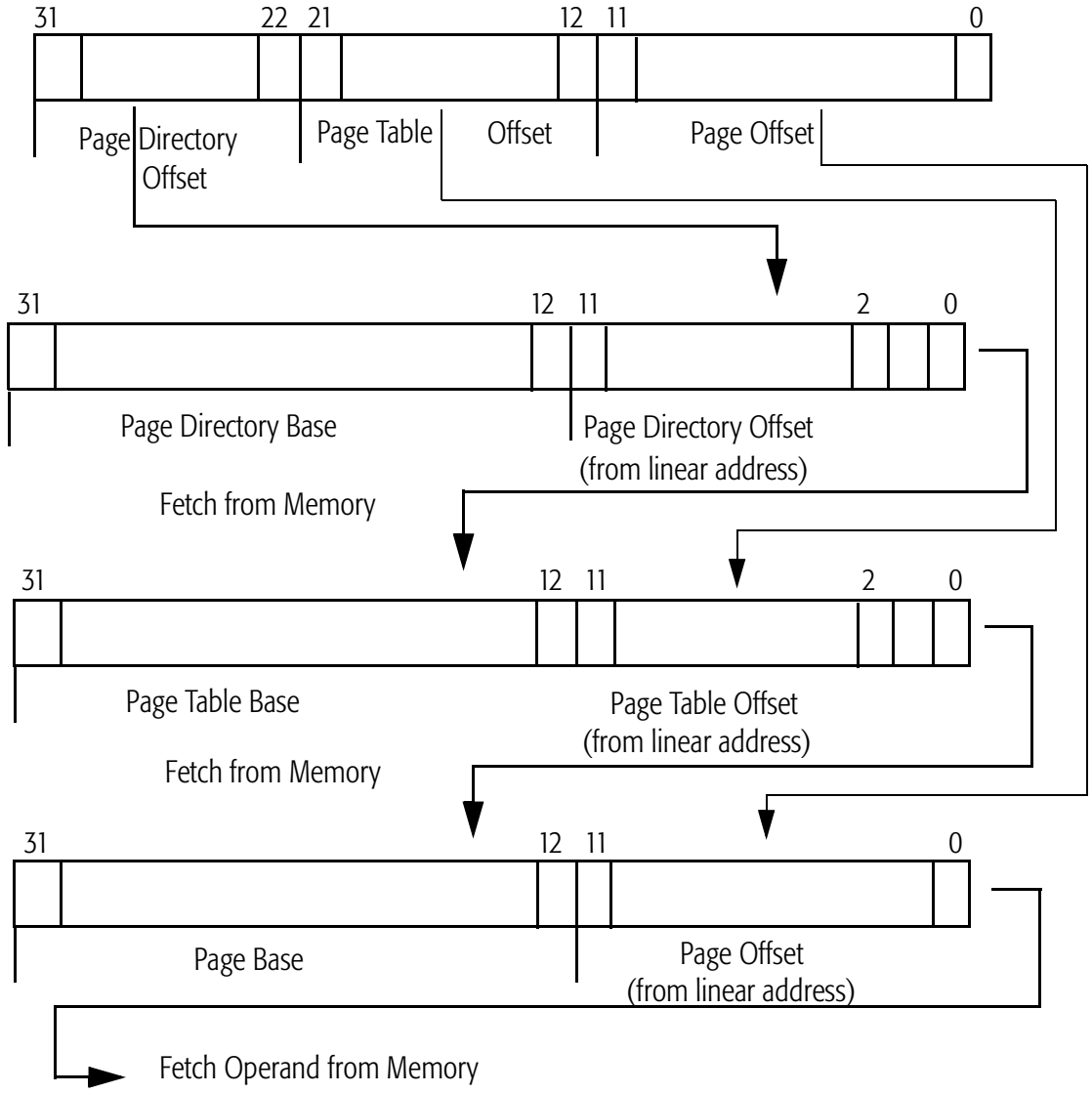


Figure 27. Two-Level GART Translation Scheme

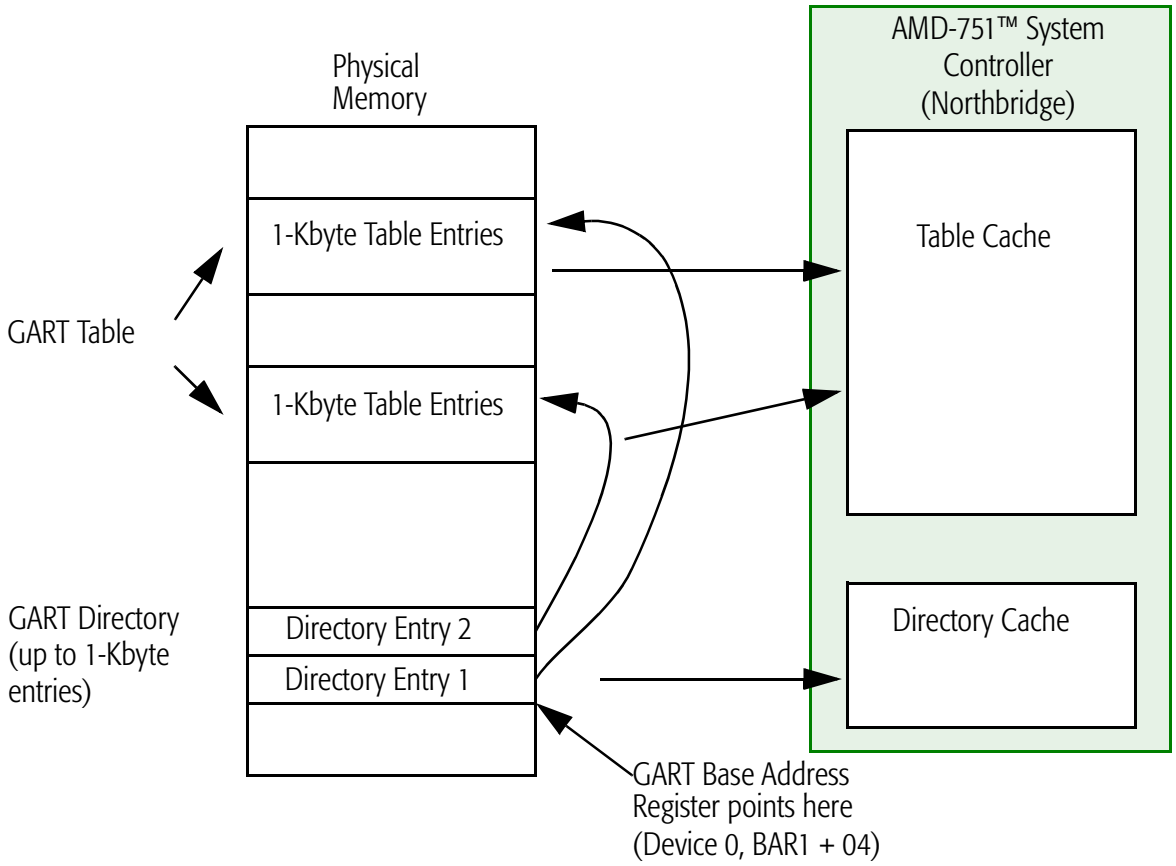


Figure 28. Another View Of the Two-Level Indexing Scheme

GTC Data

The GTC supports the referencing of a variable number of pages by one GTC entry. The GTC allows for some virtual address bits to be *selectively masked,* depending on the number of contiguous pages, before a comparison is done with the stored virtual address. Up to eight contiguous pages aligned on an eight-page boundary can be combined. The number of contiguous pages that one GTC entry can be referenced in the GTC (with the appropriate mask bits—see Table 15 on page 99) is equal to the actual number of contiguous pages approximated to the nearest lower power of 2. Therefore, if there are seven contiguous pages starting on an 8-page aligned boundary, the following conditions apply:

- The first GTC entry references four physical pages.
- The second GTC entry references two physical pages.
- The third GTC entry references one page.

In the scheme where PTEs and PDEs reference a variable number of pages, each PTE refers to a variable number of pages, depending on the number of contiguous pages starting from the page whose physical address is given by bits 31–12 of this PTE. The GTC uses this PTE to increase its hit rate.

Because the chipset miniport driver sets up the PTEs and programs the page directory of the chipset or table base address, it knows the number of contiguous pages equal to the nearest lower power of 2, starting from each page referenced by a given PTE. Software uses this number of contiguous pages to arrive at mask bits for up to three virtual address bits (14–12). These mask bits are used during virtual address comparison to mask off some or all of bits 14–12 before comparison, depending on the number of contiguous pages starting at this page. Table 15 on page 99 explains the mask bit derivation. Values other than those shown in the table are illegal. In addition, software must ensure that the first page of a contiguous block of N pages (N=2, 4, 8) is aligned on an N-page boundary.

GART Table Cache (GTC). The GTC is a fully-associative TLB with sixteen 19-bit comparators that uses tag-comparison and a least-recently used (LRU) replacement algorithm. Each entry consists of one valid bit, an 18-bit VPA, and a 20-bit PPA.

When a new VPA is available, it is compared with all 16 tag entries in parallel. If one of the 16 parallel address comparators matches and is qualified by the entry valid bit, the corresponding Hit[15:0] signal selects the correct PPA through the output multiplexer.

5.6 Power Management

The AMD-751 system controller supports the Advanced Configuration Power Interface (ACPI) Specification, On-Now, and PC 98 requirements through a handshake mechanism with the processor. The counters required for these features are contained in the AMD-756 peripheral bus controller companion device. SMM memory remapping is handled by a model-specific register in the AMD Athlon processor. See the *AMD Athlon™ BIOS Developers Guide*, order# 21656 for more information about the SMM remapping operation.

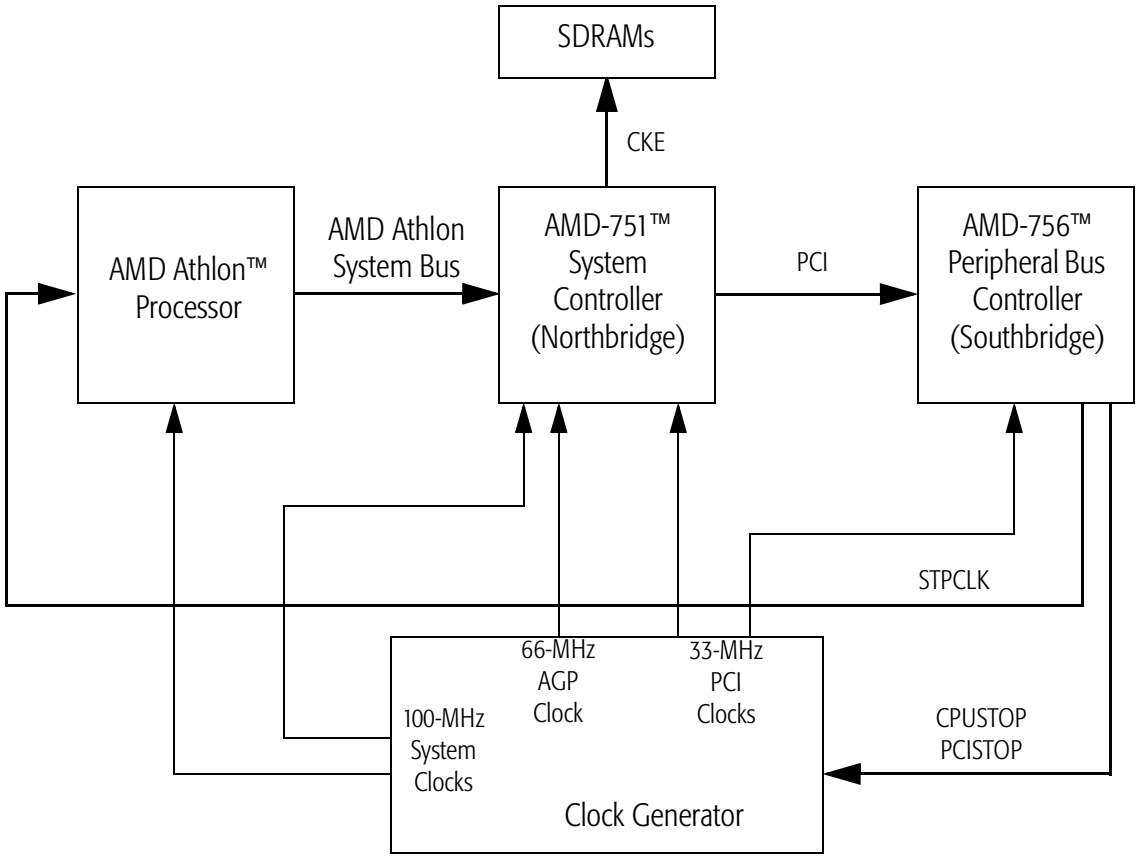


Figure 29. Power Management Signal Connections

As shown in Figure 29, the processor and the AMD-751 system controller communicate power state transitions through the AMD Athlon system bus connect/disconnect protocol and special cycles (masked writes to a defined AMD Athlon system

bus address with specific data encoding). In general, the processor initiates a request for a disconnect with a special cycle and the AMD-751 system controller may or may not actually disconnect the processor with the connect/disconnect protocol. The AMD-751 performs the requested connect/disconnect as part of the process of entering and exiting certain ACPI states. The following two special cycles are of interest:

- Halt—Generated by the AMD Athlon processor in response to executing a HALT instruction. Optionally, the AMD-751 system controller (through a configuration register bit) initiates an AMD Athlon system bus disconnect to the processor and then sends a Halt special cycle on the PCI bus. In addition, when a Halt-Disconnect occurs, the AMD-751 places the SDRAMs into self-refresh operation.
- Stop Grant—Generated by the AMD Athlon processor in response to assertion of STPCLK#. When the AMD-751 system controller receives a Stop Grant from the processor, it initiates the following sequence of actions:

  1. The AMD-751 system controller disables PCI/AGP arbitration and waits for all queues to memory to be empty (including refresh requests)
  2. The AMD-751 completes the AMD Athlon system bus cycle. The AMD-751 then initiates a AMD Athlon system bus disconnect to the processor.
  3. The AMD-751 sends a Stop Grant special cycle on the PCI bus.
  4. The AMD-756 peripheral bus controller receives and enters the appropriate power state. The AMD-756 may then assert DCSTOP#.

     Note: *The AMD-751 does not support DCSTOP#.*

Halt special cycles are generally considered part of an ACPI state definition (C1). STPCLK#, however may be asserted at random times while the processor is in the full-running state (C0), which conserves power (clock throttling).

The only programmable power management function in the AMD-751 system controller is bit 0 in PM2 (BAR2, offset 0). This bit disables arbitration when the system is powered down.

ACPI

When the processor samples STPCLK# asserted, it generates a Stop Grant special cycle. The AMD-751 passes this cycle to the PCI bus in the form of a special cycle and preserves the address during the address phase of the cycle, although the PCI specification does not require it. The the PCI Stop Grant special cycle informs the AMD-756 peripheral bus controller ACPI logic to transition to the lower-power state.

ACPI Power States

The AMD-751 system controller implements two basic power states—Full-On and Halt/Stop Grant. These states are entered and exited through special cycles from the processor. Figure 30 on page 109 shows the AMD-751 power management state machine (PMSM). The two basic power states are described in this section.

Full-On (C0). In this state the AMD-751 system controller is fully operational, all clock trees are running, and the AMD-751 provides refresh to the SDRAMs.

Halt (C1), Stop Grant (C2), and Sleep (C3). If the AMD-751 system controller detects a Halt special cycle from the processor, the Halt state (C1) is entered and the AMD-751 disconnects the processor. PCI and AGP masters continue to run (ARB_DIS clear). If the AMD-751 detects a PCI DMA master transaction that needs a snoop, the processor is connected and the probe cycle(s) run (C2). If the processor does not start any non-NOP AMD Athlon system bus cycles while the probe is in progress, the AMD-751 system controller puts the processor back to sleep (C3) following the completion of the probe. If the processor starts sending non-NOP AMD Athlon system bus cycles while connected, the AMD-751 transitions to the Full-On state.

If the AMD-751 system controller has detected a Stop Grant special cycle from the processor, the Stop Grant state is entered and the AMD-751 disconnects the processor. SDRAM is put in self-refresh mode. If software sets ARB_DIS, no DMA activity is allowed on the PCI bus and the system is in the Sleep state (C3). When the AMD-751 system controller detects that the processor wishes to wake up (PROCRDY assertion), SDRAMs are taken out of self-refresh mode and the processor is reconnected.

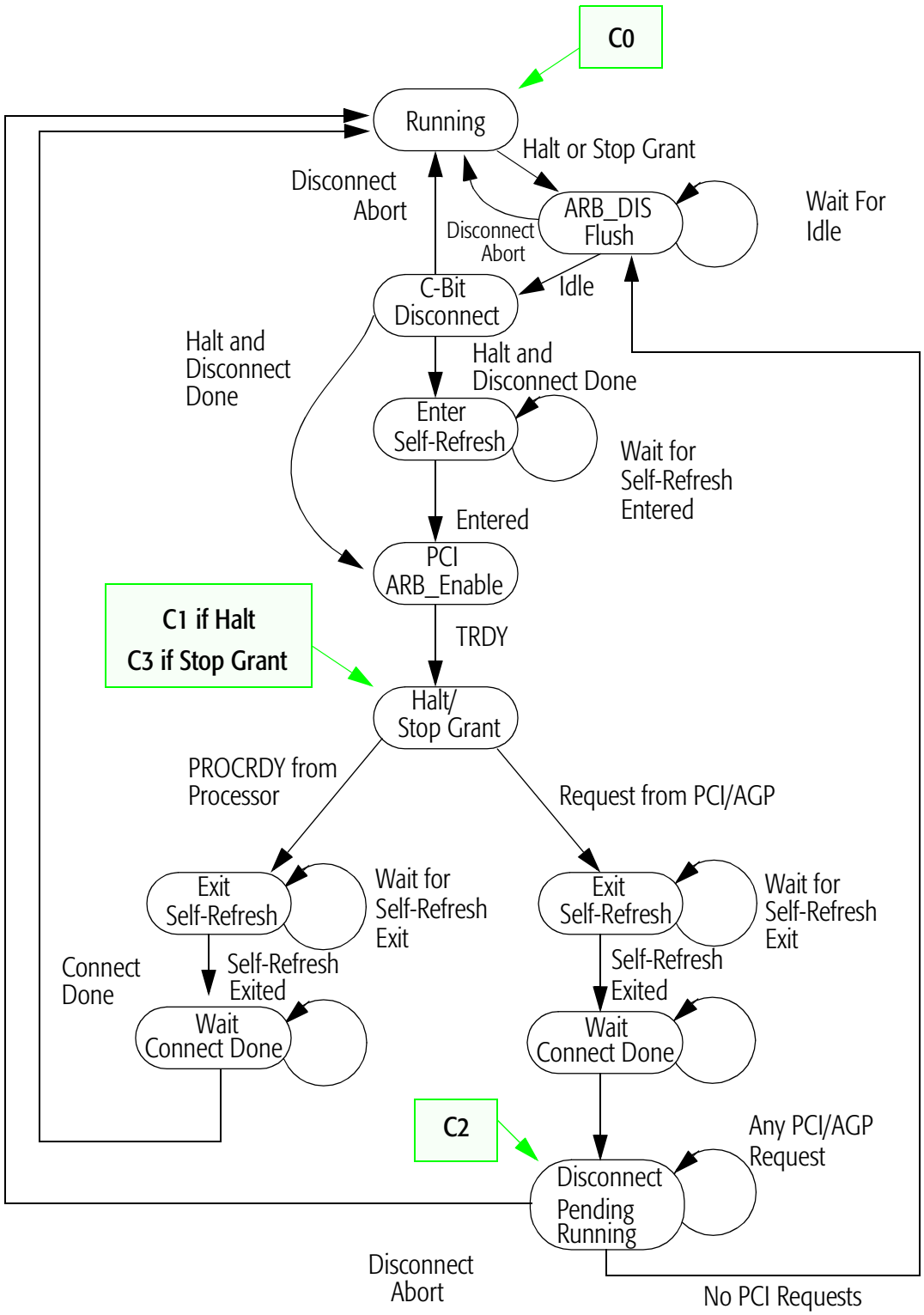


Figure 30. ACPI Power States

5.7 Phase Locked Loop (PLL) Features

The phase locked loop (PLL) has the following specifications:

- Peripheral clock (PCLK) operates at 66 MHz.
- AGP 2x clock (AGP2xCLK) operates at 133 MHz.
- Core clock (CCLK) can be switched between 100 MHz and 66 MHz, as defined by an input pin at reset. The core clock must be an integral multiple of 33 MHz.
- The two clocks (PCLK and CCLK) must have a common edge.

PLL Clock Outputs

The PLL has two output clocks that are distributed throughout the AMD-751. The peripheral clock, which runs at 66 MHz, is used by all the sequencers and logic controlling the peripheral buses (PCI and AGP). The standard PCI logic runs internally at 66 MHz. The external bus operates at half that speed, and the conversion is done with clock-enable logic at the bus interface. In addition, the AGP logic gets the 133-MHz clock it needs for the double-pumped logic. Every rising edge of the AGP 2x clock has to align with an edge of the peripheral clock (66 MHz).

The core clock is distributed throughout the AMD-751. It runs either at 100 MHz or 66 MHz, depending on the system board and external configuration. The pin that defines which of these frequencies to use is static and must not change during operation.

The PLL enables the two clocks (core clock and peripheral clock) to have a common rising edge. If the clock frequencies are 66 MHz for the peripheral and 100-MHz for the core, there is a common rising edge every three core clocks and every two peripheral clocks.

6 Typical Settings

Table 16 lists typical MSR settings for the AMD-751 system controller.

Table 16. AMD-751™ System Controller MSR Settings

Register Func:Reg	Bit	Description	BIOS Initialized Value	Setup Option Required/ Suggested	Setup Option
0:0x10	31:25	AGP base address high	xxxxb	No	AGP aperture size is selected in Dev0:0xAC[3:1] and has to be set before PCI enumeration
	24:0	Base low, prefetchable, type, memory	0008h	No	Base low (24:4) are hardwired to 0
0:0x14	31:12	GART memory mapped register base high	xxxxh	No	Assigned by PCI enumeration
	11:0	Base low, prefetchable, type, memory	008h	No	Base low (11;4) are hardwired to 0
0:0x18	31:24	Reserved	0		
	23:2	PM2_BLK I/O register base address	xxxxh	No	Assigned by PCI enumeration. Port has to be enabled by setting Dev0: 0x84[7] to "1"
	1	Reserved	0		
	0	I/O space	1	No	hardwired
0:0x40/41, 0:0x42/43, 0:0x44/45, 0:0x46/47, 0:0x48/49, 0:0x4A/4B	15:7	Bank base address [31:23] – starting address of the bank (at 8M byte boundary)	xxh	No	According to memory installed

Table 16. AMD-751™ System Controller MSR Settings (Continued)

Register Func:Reg	Bit	Description	BIOS Initialized Value	Setup Option Required/ Suggested	Setup Option
	6:1	Bank address mask [28:23]	xh	No	Used as the size of a bank 000001 – 8M 000011 – 16M 000111 – 32M 001111 – 64M 011111 – 128M 111111 – 256M
	0	Bank enable	x	No	0 – if memory is not present 1 – if memory is present
0:0x50, 0:0x51, 0:0x52	7	Reserved	0h		
	6	Bank(x+1) address mode	X	No	0 – 16Mbit x4, x8, x16 1 – 64Mbit x4, x8, x16
	5	Number of banks in bank(x+1) (internal DRAM banks on a DIMM)	x	No	0 – 2 banks 1 – 4 banks
	4:3	Reserved	00		
	2	Bank(x) address mode	x	No	0 – 16Mbit x4, x8, x16 1 – 64Mbit x4, x8, x16
	1	Number of banks in bank (x) (internal DRAM banks on a DIMM)	x	No	0 – 2 banks 1 – 4 banks
	0	Reserved	0		
0:0x54	31:25	Reserved			
	24	Idle Cycle Limit bit 2	0	No	See bit[13:12]
	23:22	SDRAM AddrB Drv ClkOut Drv	xxb	Yes	00 – low 01 – medium low 10 – medium high 11 – high

Table 16. AMD-751™ System Controller MSR Settings (Continued)

Register Func:Reg	Bit	Description	BIOS Initialized Value	Setup Option Required/ Suggested	Setup Option
	21:20	SDRAM AddrA Drv	xxb	Yes	00 – low 01 – medium low 10 – medium high 11 – high
	19:18	SDRAM CAS[2:0], RAS[2:0], WE[2:0], CKE[2:0], CS[5:0] drive	xxb	Yes	00 – low 01 – medium low 10 – medium high 11 – high
	17:16	SDRAM DQM drive	1	Yes	00 – low 01 – medium low 10 – medium high 11 – high
	15:14	Page Hit request before a non-Page Hit	10	No	00 – 1cyc, 01 – 4cyc 10 – 32cyc, 11 – 64cyc
	13:12	Idle cycle to wait before precharging the idle bank	01	No	000 – 0 cyc 001 – 8 cyc (deflt) 010 – 12 cyc 011 – 16 cyc 100 – 24 cyc 101 – 32 cyc 110 – 48 cyc 111 – rsvd
	11:9	Trc timing value	101	No	000 – 3cyc, 001 – 4cyc 010 – 5cyc, 011 – 6cyc 100 – 7cyc, 101 – 8cyc 110 – rsvd, 111 – rsvd
	8:7	Trp timing	00	No	00 – 3cyc, 01 – 2cyc, 1x – 1cyc
	6:4	Tras timing	101	No	000 – 2cyc 001 – 3cyc 010 – 4cyc 011 – 5cyc 100 – 6cyc 101 – 7cyc 110 – rsvd 111 – rsvd
	3:2	Tcl (CAS latency)	00	Yes	00 – 3cyc 01 – 2cyc 10 – rsvd 11 – 4cyc

Table 16. AMD-751™ System Controller MSR Settings (Continued)

Register Func:Reg	Bit	Description	BIOS Initialized Value	Setup Option Required/ Suggested	Setup Option
	1:0	Trcd (RAS to CAS latency)	10	Yes	00 – 1cyc 01 – 2cyc 10 – 3cyc 11 – 4cyc
0:0x58	31:26	Reserved			
	25	SDRAM init	1	No	
	24	SDRAM type (reserved for future use) 0 – SDRAM, 1 – ESDRAM	0	No	ESDRAM is not supported by the AMD-751 system controller
	23	Mode register status (read/write once) 0 – off/done, 1– to set	0	No	
	22:21	Reserved	00b		
	20	Burst refresh enable 0 – no bursting refreshing, 1 – queue up to 4 refreshes before issuing	0	Yes	
	19	Largest burst length (for future use) 0 – 8QW 1 – 4QW	0	No	
	18	ECC enable 0 – disable 1 – enable	0	Yes	Disabled by default
	17:16	Refresh counter 00 – 2K cycle 01 – 1.5K cycle 10 – 1K cycle 11 – 512K cycle	00b	No	
	15:10	Reserved	000000b		
	9:8	ECC status 00 – no error 01 – multi-bit error (SERR) 10 – single-bit error detected 11 – single and multi-bit error (SERR)	00b	No	
	7:6	Reserved	00b		

Table 16. AMD-751™ System Controller MSR Settings (Continued)

Register Func:Reg	Bit	Description	BIOS Initialized Value	Setup Option Required/ Suggested	Setup Option
	5:0	One hot encoded chipselect of request that generate the single or multi-bit error	00000b	No	
0:0x60	31	Probe enable for CPU0 (0 – disable, 1 – enable)	1	No	
	30	Lck Half C2M	0	No	
	29	Lck Half M2C	0	No	
	28	Lck Half Prb	0	No	
	27:25	Xca Probe Count	010b	No	Default
	24:22	Xca Read Count	110b	No	Default
	21:19	Xca Write Count	100b	No	Default
	18	Halt disconnect enable 0 – no AMD Athlon system bus disconnect following HALT 1 – perform AMD Athlon system bus disconnect after HALT	0	Yes	Setup item is for debugging only
	17	Stop grant disconnect enable 0 – no AMD Athlon system bus disconnect following STOPGRANT 1 – perform AMD Athlon system bus disconnect after STOPGRANT	1	No	
	16:14	Probe limit 000 – 1 probe 001 – 2 probes …. 110 – 7 probes 111 – 8 probes (max)	111b	No	111b

Table 16. AMD-751™ System Controller MSR Settings (Continued)

Register Func:Reg	Bit	Description	BIOS Initialized Value	Setup Option Required/ Suggested	Setup Option
	13:10	Ack limit 0000 – 1 un0acked command 0001 – 2 …. 1111 –- 16	0011b		Read only Processor SysAckLimit = Ack_Limit + 1
	9	Bypass Enable 1 – System controller bypasses certain memory to processor pipe stages for optimal performance	0	Yes	
	8:7	SysDCOut delay 00 – rsvd 01 – 1 Clk 10 – 2 Clks 11 – 3 Clks	10b		Read only
	6:3	SysDCIn delay	1010b	No	Read only
	2	WR2RD	0	No	Read only
	1:0	RD2WR	10b	No	Read only
0:0x64	31	ClkFwd Offset 0 – AMD-751 system controller delays assertion of data and clock for AMD Athlon system bus SysData 1 – no delay	0	No	
	30:0	All Read Only bits	52321824h	No	Read only
0:0x68		BIU1 status/control (not used)	00000000h	No	
0:0x6C		BIU1 SIP (not used)	00000000h	No	
0:0x70	31:11	Reserved	0	No	

Table 16. AMD-751™ System Controller MSR Settings (Continued)

Register Func:Reg	Bit	Description	BIOS Initialized Value	Setup Option Required/ Suggested	Setup Option
	10	PCI pipe enable 0 – MRO checks outstanding read probe before PCI transactions 1 – MRO pipelines PCI transactions	1	No	Always set
	9	PCI Block Write Enable 0 – BIU performs RID/INV probes, forcing MRO MWQ to wait for data movement 1 – BIU performs NOP/INV probes for PCI full-block writes	1	No	Always set
	8:6	Arbitration mode (testing only)	000b	No	
	5:2	Memory Read Queue Disable (testing only)	0000b	No	
	1	Memory Write Queue Disable (testing only)	0	No	
	0	Reorder disable 0 – MRO reorders memory requests to optimize memory performance 1 – no reordering	0	No	
0:0x80	31:18	Reserved	0		
	17	BIU1 present	0		Read only
	16	BIU0 present	1		Read only
	15:8	First AMD Athlon system bus ID	00h		Read only
	7:0	Who AM I	00h		Read only

Table 16. AMD-751™ System Controller MSR Settings (Continued)

Register Func:Reg	Bit	Description	BIOS Initialized Value	Setup Option Required/ Suggested	Setup Option
0:0x84	31:24	AGP VGA BIOS address decode Bit31: 0D_C000 – 0D_FFFF Bit30: 0D_8000 – 0D_BFFF … Bit24: 0C_0000 – 0C_3FFF	00h	No	
	23:18	Reserved	000000b		
	17	Enable APC chaining 1 – processor writes to APC are chained together	1	Yes	
	16	Enable PCI chaining 1 – processor writes to PCI are chained together	1	Yes	
	15	MDA support	x	Yes	If MDA is present and AGP is present
	14	PCI Write-Post retry 0 – no retry 1 – enables retry on PCI if there are pending posted write	0	No	
	13	APCI Write Post retry 0 – no retry 1 – enables APCI if there are pending posted write	0	No	
	12	Dis Rd Data Err 0 – returns read data error to processor on master abort or target abort 1 – AMD-751 system controller returns all ones on data read error	1	No	

Table 16. AMD-751™ System Controller MSR Settings (Continued)

Register Func:Reg	Bit	Description	BIOS Initialized Value	Setup Option Required/ Suggested	Setup Option
	11	Dis APC Early Probe 1 – disable early snoop from AGP master running a PCI cycle to memory	0	No	
	10	Dis PCI Early Probe 1 – disable early probe request for write cycles from an external PCI master	0	No	
	9	Dis AGP arbiter pipelining 1 – disable AGP arbiter from pipelining grants onto bus	0	No	
	8	Southbridge lock disable 1 – disable flushing function performed before granting bus to the SB.	0	No	
	7	PM register enable 1 – enables R/W accesses to PM register at 0:0x18	1	No	ACPI required
	6	15M hole enable 0 – disable memory hole at 15–16M 1 – enable a memory hole at 15–16M	0	Yes	
	5	14M hole enable 0 – disable memory hole at 14–15M 1 – enable a memory hole at 14–15M	0	Yes	
	4	EV6 mode 1 – enable PCI decoding in EV6 mode	0	No	May be enabled to allow DMA transfer at A0000–FFFFF

Table 16. AMD-751™ System Controller MSR Settings (Continued)

Register Func:Reg	Bit	Description	BIOS Initialized Value	Setup Option Required/ Suggested	Setup Option
	3	Target latency timer disable 1 – disable AMD-751 system controller target latency timer on both PCI and AGP's PCI interfaces	0	No	
	2	ApcPreEn 1 – enables AMD-751 to prefetch data from SDRAM when a PCI master on AGP bus reads from main memory	1	No	
	1	PciPreEn 1 – enables AMD-751 system controller to prefetch data from SDRAM when a PCI master on PCI bus reads from main memory	1	No	
	0	ParkPCI 0 – PCI arbiter parks on processor accesses to PCI 1 – enables parking on an external PCI master	1	No	
0:0x88	31:0	Config Status	02410004h		Read only
0:0xA0	31:0	AGP Capability Identifier Register	00100002h		Read only
0:0xA4	31:0	AGP Status Register	0f000203h		Read only
0:0xA8	31:10	Reserved			
	9	Sideband addressing enable 0 – disable 1 – enable	0	No	
	8	AGP operation enable 0 – AGP operation ignored 1 – enable AGP operation	0	Yes	

Table 16. AMD-751™ System Controller MSR Settings (Continued)

Register Func:Reg	Bit	Description	BIOS Initialized Value	Setup Option Required/ Suggested	Setup Option
	7:6	Reserved	0		
	5	Greater than 4G address support 0 – disable 1 – enable	0	No	
	4:2	Reserved			
	1:0	AGP data transfer mode 01b – 1x 10b – 2x	0	No	Power on default
0:0xAC	31:17	Reserved	000h		
	16	VGA ISA address decoding 0 – no ISA aliasing on address [15:0] 1 – force AMD-751 system controller to alias ISA address [15:0]	1	Yes	
	15:4	Reserved	000h		
	3:1	AGP aperture size 000 – 32MB 001 – 64MB 010 – 128MB 011 – 256MB 100 – 512MB 101 – 1GB 110 – 2GB	000b	Yes	
	0	AGP aperture base address enable 0 – disable register 0:0x10 (BAR0) 1 – enable register 0:0x10 (BAR0)	0	Yes	1 – if AGP is enabled in setup page
0:0xB0	31:21	Reserved			
	20	AGP Read Buffer Size 0 – 64QW 1 – 32QW	0	No	

Table 16. AMD-751™ System Controller MSR Settings (Continued)

Register Func:Reg	Bit	Description	BIOS Initialized Value	Setup Option Required/ Suggested	Setup Option
	19	Non-GART Snoop 0 – AGP address falling outside GART do not cause probes 1 – enable probes	0	No	
	18	Post GART queue size 0 – 8 entries 1 – 4 entries	0	No	
	17	GART page directory cache enable 0 – disable 1 – enable	0	No	
	16	GART Index Scheme control 0 – Two-level mode 1 – One-level mode	0	No	
	15:8	Reserved			
	7	Processor/AGP Read/Write sync enable 0 – no synchronization 1 – AMD-751 system controller ensures that all writes to GART range from processor to memory are retired before initiating processor-to-AGP cycle	0	No	
	6:0	Reserved			
1:0x00 ~ 1:0x3F		PCI to PCI bridge config spaces BIOS assigns this P-to-P bridge as bus 1 and sets memory and I/O base/limit according to P-to-P bridge spec if AGP video is installed		No	

7 Configuration Registers

All of the many options available on the AMD-751 system controller are selected by writing to its PCI configuration registers. These registers are usually programmed during system initialization and are not accessed during normal operation. However, some registers may require specific programming sequences during power-on self-test (POST) to detect the type and size of installed memory.

This section provides a description of the mechanism used to access the AMD-751 PCI configuration registers as well as the location and functional details of each register.

7.1 PCI Configuration Mechanism

The AMD-751 system controller uses PCI configuration mechanism #0 or #1 to convey and receive configuration data to and from the AMD Athlon processor. These mechanisms, described in *PCI Local Bus Specification, Revision 2.2*, employ I/O locations 0CF8h–0CFBh (address 1F_C000_0CF8h) to specify the target address and I/O locations 0CFCh–0CFFh (address 1F_C000_0CFCh) for data to or from the target address. The target address includes the PCI bus, device, function, and register numbers of the PCI device.

The AMD-751 system controller implements most registers as PCI configuration registers. x86 software executes IN and OUT instructions to I/O addresses of 0CF8h and 0CFCh to access all configuration registers, which are translated by the processor into AMD Athlon system bus RdBytes and WrBytes commands, with the lower 24 bits of the address field containing the logical contents of the ConfigAddr register (I/O address 0CF8h).

Configuration accesses in the AMD-751 system controller conform to the following rules:

- The AMD-751 is defined to be device 0. The IDSEL pin on every external PCI device must be wired to one of the AD[31:12] lines, because logically AD[11] is assigned to device 0.
- Device 0 accesses correspond to the Processor-to-PCI bridge registers listed in Table 18 on page 126 and defined starting on page 130.
- Device 1 accesses correspond to the PCI-to-PCI bridge registers listed in Table 19 on page 128 and defined starting on page 161.

- Accesses can be byte, word, or doubleword in length and must be naturally aligned.

The AMD-751 system controller creates type 0 and type 1 accesses as follows:

- If SysAddOut[23:16] = 0 (Bus number = 00h), a type 0 configuration cycle is generated and PCI AD[1:0] = 00b. Device number, SysAdd[15:11] is decoded and asserted on PCI AD[31:11] for IDSEL.
- If SysAddOut[23:16] is not = 0 (Bus number = 00h), a type 1 configuration cycle is generated and PCI AD[1:0] = 01b. Bus number and device number fields are passed onto the PCI directly with no decoding. PCI AD[31:24] = 00h.

Configuration Address — Ports 0CFBh–0CF8h

31	Bit 30 – Bit 24	Bit 23 – Bit 16	Bit 15 – Bit 11	10 – 8	Bit 7 – Bit 2	1	0
En	Reserved	Bus Number	Device Number	Function #	Register Number	0	0
I/O Address OCFBh		I/O Address OCFAh	I/O Address OCF9h		I/O Address OCF8h		

Configuration address is a read-write port that responds only to doubleword accesses. Byte or word accesses are passed on unchanged.

Bit 31 **Configuration Space Enable**—Bit 31 enables the AMD-751 configuration space.

1 = The targeted PCI device responds
0 = The I/O access is passed on unchanged

Bits 30–24 **Reserved** (always reads 0)

Bits 23–16 **PCI Bus Number**—These bits select a specific system PCI bus. The AMD-751 only supports one logical PCI bus.

Bits 15–11 **Device Number**—This field defines which device is to be accessed in the system on the target PCI bus. For type #0 configuration cycles, the AMD-751 system controller decodes this field and asserts the appropriate AD signal during the address phase to select the defined device. For type #1 configuration cycles, the AMD-751 passes this field through to the AD bus undecoded to select the defined device. Devices are assigned a number by tying the device IDSEL# pin to a PCI AD line. The AMD-751 system controller uses device 0 and device 1, which correspond to AD11 and AD12, respectively. Device 0 (00000b) is the standard Processor-to-PCI bridge registers. Device 1 (00001b) is the PCI-to-PCI bridge register set used to access the AGP registers.

Note: *AD11 and AD12 are reserved for the AMD-751 system controller and should not be accessed as IDSEL signals by any other PCI device.*

Bits 10–8 **Function Number**—These bits select the number of a specific function. The AMD-751 system controller is Function 0.

Bits 7–2 **Register Number**—These bits specify the offset number of a register within the selected device space. The register number is a doubleword that, in conjunction with the PCI byte enable lines C/BE[3:0]#, specifies the configuration register offset number.

Bits 1–0 **Reserved** (always reads 0)

Configuration Data — Ports 0CFFh–0CFCh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
xxxxxxxxh																															

Configuration data is a read-write port that responds only to doubleword accesses. Byte or word accesses are passed on unchanged.

Note: *In the AMD-751 system controller, IDSEL is internally connected to AD11. Other PCI devices in a system must connect their IDSEL lines to a unique line in AD[31:12] and cannot use AD11.*

Table 17 summarizes the I/O ports involved in PCI configuration.

Table 17. Configuration Port Register Summary

Register Name	I/O Address	Type	Default Value	Size
IO_CNTRL	0CF8h	R/W	0000 0000h	32
IO_DATA32	0CFCh	R/W	0000 0000h	32
IO_ODD_DATA16	0CFCh	R/W	0000h	16
IO_EVEN_DATA16	0CFEh	R/W	0000h	16
IO_0_DATA8	0CFCh	R/W	00h	8
IO_1_DATA8	0CFDh	R/W	00h	8
IO_2_DATA8	0CFEh	R/W	00h	8
IO_3_DATA8	0CFFh	R/W	00h	8

7.2 Register Overview

Table 18 through Table 20 summarize the AMD-751 system controller configuration register offsets, devices, default values after reset, and access types. Access types are indicated as follows:

- RW Read/Write
- RO Read Only
- RWC Read and/or write 1's to clear individual bits
- RWS Read, but can only write a 1 to set the bit (a 0 does not reset the bit)
- RW0 Read and Write only 0's for proper operation

Table 18. Function 0, Device 0 Configuration Registers

Offset	Cache Control	Reset	Access	Description
01h–00h	Vendor ID (AMD)	1022h	RO	page 130
03h–02h	Device ID Single Processor Device	7006h	RO	page 130
05h–04h	Command	0004h	RW	page 130
07h–06h	Status	0210h	RWC	page 131
08h	Revision ID	nn *	RO	page 133
09h	Programming Interface	00h	RO	page 133
0Ah	Subclass Code	00h	RO	page 133
0Bh	Base Class Code	06h	RO	page 133
0Ch	Reserved	00h	RO	page 133
0Dh	Latency Timer	00h	RW	page 134
0Eh	Header Type	80h	RO	page 134
0Fh	Reserved	00h	RO	
13h–10h	Base Address 0 (BAR0) (AGP Memory)	0000_0008h	RW	page 135
17h–14h	Base Address 1 (BAR1) (GART Registers)	0000_0008h	RW	page 136
1Bh–18h	Base Address 2 (BAR2) (PM2)	0000_0001h	RW	page 136
37h–34h	Capabilities	0000_00A0h	RO	page 137
41h–40h	Base Address Chip Select 0	0000h	RW	page 137
43h–42h	Base Address Chip Select 1	0000h	RW	page 138
45h–44h	Base Address Chip Select 2	0000h	RW	page 138
47h–46h	Base Address Chip Select 3	0000h	RW	page 138

Note:

* *nn changes for each device revision. For example, 00h = Revision A, Stepping 1; 01h = Revision A, Stepping 2; 10h = Revision B, Stepping 1; 21h = Revision C, Stepping 2; etc.*

Table 18. Function 0, Device 0 Configuration Registers (Continued)

Offset	Cache Control	Reset	Access	Description
49h–48h	Base Address Chip Select 4	0000h	RW	page 139
4Bh–4Ah	Base Address Chip Select 5	0000h	RW	page 139
50h	SDRAM Address Mapping 1/0	00h	RW	page 140
51h	SDRAM Address Mapping 3/2	00h	RW	page 140
52h	SDRAM Address Mapping 5/4	00h	RW	page 141
53h	Reserved	00h	RO	
55h–54h	DRAM Timing	0000h	RW	page 143
57h–56h	DRAM CS Driver Strength	0000h	RW	page 144
59h–58h	DRAM ECC Status	00h	RW	page 145
5Bh–5Ah	DRAM Mode/Status	00h	RW	page 146
63h–60h	BIU Status and Control	0000_0Cxxh	RW	page 147
67h–64h	BIU SIP	0000_0000h	RW	page 149
69h–68h	BIU Status 1 (Reserved)	000xh	RW	page 150
6Bh–6Ah	Reserved	0000h	RW	
6Fh–6Ch	Reserved	0000_0000h	RW	
71h–70h	MRO Control Register	0001h	RW	page 150
81h–80h	Who Am I (WHAMI)	00xxh	RW	page 151
83h–82h	Reserved	0000h	RO	
85h–84h	PCI Arbitration Control	0000h	RW	page 151
86h	PCI and APCI Chaining	00h	RW	page 154
87h	AGP VGA BIOS Mask	00h	RW	page 154
89h–88h	Config/Status #1	0x0xh	RW	page 155
8Bh –8Ah	Config/Status #2	000xh	RW	page 155
A3h–A0h	AGP Capability Identifier	0100_0002h	RO	page 156
A7h–A4h	AGP Status	0F00_0203h	RO	page 157
ABh–A8h	AGP Command	0000_0000h	RW	page 158
AFh–ACh	AGP Virtual Address Space Size	0001_0000h	RW	page 158
B0h	AGP Mode Control Register #1	00h	RW	page 159
B2h	AGP Mode Control Register #2	02h	RW	page 160

Note:

* *nn changes for each device revision. For example, 00h = Revision A, Stepping 1; 01h = Revision A, Stepping 2; 10h = Revision B, Stepping 1; 21h = Revision C, Stepping 2; etc.*

Table 19. Function 0, Device 1 Configuration Registers

Offset	PCI Header	Reset	Access	Description
01h–00h	Vendor ID	1022h	RO	page 161
03h–02h	Device ID	7007h	RO	page 161
05h–04h	AGP/PCI Command	0000h	RW	page 161
07h–06h	Status	0220h	RO	page 163
08h	AGP Revision ID	00h	RO	page 164
09h	Programming Interface	00h	RO	page 164
0Ah	Subclass Code	04h	RO	page 164
0Bh	Base Class Code	06h	RO	page 164
0Ch	Reserved	00h	RO	
0Dh	Reserved	00h	RO	
0Eh	Header Type	81h	RO	page 165
0Fh	Reserved	00h	RO	
18h	Primary Bus Number	00h	RW	page 165
19h	Secondary Bus Number	00h	RW	page 165
1Ah	Subordinate Bus Number	00h	RW	page 165
1Bh	Secondary Latency Timer	00h	RW	page 166
1Ch	I/O Base Register	FFh	RW	page 166
1Dh	I/O Limit Register	0Fh	RW	page 166
1Fh–1Eh	AGP/PCI Secondary Status	0220h	RWC	page 167
21h–20h	Memory Base	0000h	RW	page 168
23h–22h	Memory Limit	0000h	RW	page 168
25h–24h	AGP/PCI Prefetchable Memory Base	0000h	RW	page 169
27h–26h	AGP/PCI Prefetchable Memory Limit	0000h	RW	page 169
30h	I/O Base	00h	RW	page 169
32h	I/O Limit	00h	RW	page 170
37h–34h	Reserved	0000_0000h	RO	
3Dh–3Ch	Interrupt Control	0000h	RW	page 170
3Fh–3Eh	PCI-to-PCI Bridge Control	0000h	RW	page 171

Table 20. Memory Space Configuration Registers (BAR1 + n)

Offset	PCI Header	Reset	Access	Description
01h–00h	Features and Capabilities	0301h	RO	page 173
03h–02h	Enable and Status	0000h	RO	page 174
07h–04h	AGP GART Base Address	0000_0000h	RW	page 175
0Bh–08h	GART Cache Size	0000_0010h	RO	page 175
0Fh–0Ch	GART Cache Control	0000_0000h	RW	page 176
13h–10h	GART Entry Control	0000_0000h	RW	page 176

Table 21. Power Management Configuration Registers (BAR2 + n)

Offset	PCI Header	Reset	Access	Description
01h–00h	PM2 (Power Management)	0000h	RW	page 177

7.3 Function 0, Device 0 Registers (Processor-to-PCI Bridge, Memory Controller, etc.)

Vendor ID — Device 0 — Offset 01h–00h

	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
	Vendor ID															
Reset	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0

This read-only value is defined as 1022h.

Device ID — Device 0 — Offset 03h–02h

	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
	Device ID															
Reset	0	1	1	1	0	0	0	0	0	0	0	0	0	1	1	0

This read-only value of 7006h represents the AMD-751 system controller single processor device.

Command — Device 0 — Offset 05h–04h

	Bits 15–10						9	8	7	6	5	4	3	2	1	Bit 0
	Reserved						FBBCE	SERRE	STEP	PER	VGAPS	MWIC	SCMON	ITEN	MEMSPC	IOSPC
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits 15–10 Reserved (always reads 0)

Bit 9 **Fast Back-to-Back Cycle Enable (always reads 0)**—Fast back-to-back cycles are not supported.

0 = Fast back-to-back transactions only allowed to the same agent

Bit 8 **SERR# Enable (RW)**—This bit does not affect the setting of bit 14 in offset 07h–06h.

0 = SERR# output driver disabled (default)
1 = SERR# output driver enabled

Note: *If a system error is detected, SERR# can be asserted by either the PCI master or the AMD-756 peripheral bus controller.*

Bit 7 Address/Data Stepping (always reads 0)

0 = Device never uses stepping

Bit 6 Parity Error Response Enable (always reads 0)

0 = Do not report parity errors in status register offset 06 bit 8 (default)
1 = Enable PCI parity response in status register offset 06 bit 8 (not supported)

Bit 5 VGA Palette Snoop (always reads 0)

0 = Palette accesses generate normal PCI cycles

Bit 4 Memory Write-and-Invalidate Command (always reads 0)—This feature increases overall performance by eliminating cache writebacks when a PCI initiator writes to the address of a modified line.

0 = The AMD-751 system controller never generates MWI. The AMD-751 responds to MWI commands by generating the appropriate probe on the AMD Athlon system bus.

Bit 3 Special Cycle Monitoring (always reads 0)

0 = Special cycles not monitored

Bit 2 Initiator Enable (always reads 1)

1 = AMD-751 system controller can behave as bus initiator

Bit 1 Memory Space (RW)

0 = Disable PCI memory space (default)
1 = Responds to PCI memory space accesses

Bit 0 I/O Space (always reads 0)—The AMD-751 does not act as an I/O target.

Status — Device 0 Offset 07h–06h

	Bit 15	14	13	12	11	10–9	8	7	6	5	4	Bits 3–0
	DPE	SERR#	RIA	RTA	STA	DEVSEL# Timing	PPE	FBBC	UDF	66 MHz	CL	Reserved
Reset	0	0	0	0	0	0 1	0	0	0	0	1	0 0 0 0

Bit 15 DRAM Parity Error Detected (always reads 0)—The AMD-751 does not support parity checking.

Bit 14 SERR# Error (RWC)—This bit is set whenever the AMD-751 system controller generates a system error and asserts SERR#.

0 = No error signaled
1 = SERR# error signaled. The AMD-751 has asserted the SERR# pin (MBE, GART error, or SERR# assertion on the AGP bus).

Bit 13 **Received Initiator Abort (RWC)**—This bit is set by a PCI initiator when its transaction is terminated with initiator abort.

0 = PCI transactions proceeding normally
1 = The AMD-751 system controller has detected that a transaction was terminated before completion

Bit 12 **Received Target Abort (RWC)**—The target issues a target abort when it detects a fatal error or cannot complete a transaction. This bit is set by simultaneously deasserting DEVSEL# and asserting STOP#.

0 = No abort received
1 = Transaction aborted by target

Bit 11 **Signaled Target Abort (always reads 0)**—The AMD-751 system controller does not report target aborts.

Bits 10–9 **DEVSEL# Timing (always reads 01)**—This field indicates that the slowest DEVSEL# timing is medium.

Bit 8 **PCI Parity Error Detected (always reads 0)**—The AMD-751 does not support parity checking.

0 = No parity error detected/Not supported

Bit 7 **Fast Back-to-Back Capability (always reads 0)**—The AMD-751 can accept fast back-to-back transactions only if they are from the same agent.

Bit 6 **User-Defined Features (always reads 0)**—The AMD-751 does not support user-defined features**.**

Bit 5 **66 MHz-Capable PCI Bus (always reads 0)**—The AMD-751 system controller only supports the 33-MHz PCI bus.

0 = 33-MHz PCI bus support (default)
1 = 66-MHz PCI bus support (not supported)

Bit 4 **Capabilities List (always reads 1)**—This bit indicates that the configuration space of this device contains a capabilities list.

Bits 3–0 **Reserved (always reads 0)**

Revision ID — Device 0 Offset 08h

	Bit 7	6	5	4	3	2	1	Bit 0
	AMD-751 System Controller Chip Revision and Stepping Code							
Reset	–	–	–	–	–	–	–	–

Bits 7–0 **AMD-751™ System Controller Revision Code (RO)**—The most-significant nibble indicates the die revision and the least-significant nibble represents the stepping. (For example, 00h = Revision A, Stepping 1; 01h = Revision A, Stepping 2; 10h = Revision B, Stepping 1; 21h = Revision C, Stepping 2; etc.)

Programming Interface — Device 0 Offset 09h

	Bit 7	6	5	4	3	2	1	Bit 0
	Programming Interface							
Reset	0	0	0	0	0	0	0	0

Bits 7–0 **AMD-751 System Controller Programming Interface (always reads 00h)**—This register is defined in different ways for each combination of base and subclass codes. It is undefined for this type of device.

Subclass Code — Device 0 Offset 0Ah

	Bit 7	6	5	4	3	2	1	Bit 0
	Subclass Code							
Reset	0	0	0	0	0	0	0	0

Bits 7–0 **Subclass Code (always reads 00h)**—The PCI-defined subclass code for a processor bridge is 00h.

Base Class Code — Device 0 Offset 0Bh

	Bit 7	6	5	4	3	2	1	Bit 0
	Base Class Code							
Reset	0	0	0	0	0	1	1	0

Bits 7–0 **Base Class Code (always reads 06h)**—The PCI-defined base class code for a bridge device is 06h.

Reserved — Device 0 Offset 0Ch

	Bit 7	6	5	4	3	2	1	Bit 0
	Reserved							
Reset	0	0	0	0	0	0	0	0

Bits 7–0 **Reserved (always reads 00h)**

Latency Timer — Device 0 Offset 0Dh

	Bit 7	6	5	4	3	2	1	Bit 0
	Latency Timer Values							
Reset	0	0	0	0	0	0	0	0

Bits 7–0 **Latency Timer Value (RW)**—This 8-bit binary value specifies the latency timer in units of PCI bus clocks.

00000000 = 0 PCI clocks
00000001–11111111 = (8-bit binary value) x PCI clocks

Header Type — Device 0 Offset 0Eh

	Bit 7	6	5	4	3	2	1	Bit 0
	Header Type							
Reset	1	0	0	0	0	0	0	0

Bits 7–0 **PCI Header Type (RO)**—The AMD-751 system controller PCI header type is 80h, indicating a multifunction device.

Reserved — Device 0 Offset 0Fh

	Bit 7	6	5	4	3	2	1	Bit 0
	Reserved							
Reset	0	0	0	0	0	0	0	0

Bits 7–0 **Reserved (always reads 00h)**

Base Address Register 0 (BAR0) Device 0 Offset 13h–10h

	Bits 31–25	Bits 24–4	Bit 3	Bits 2–1	Bit 0
	Size	Base Address Low	Pre	Type	Mem
Reset	0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1	0 0	0

This register is used by system BIOS memory mapping firmware to allocate virtual address space for AGP.

Bits 31–25 Size (RW) (default = 000000b)—BIOS firmware writes 1s to this field, then reads the field back to determine how much memory is required for AGP. The meaning of the returned value, shown in Table 22, is a memory allocation size identical to the value represented in Device 0, Offset ACh, bits 3–1. (see page 159).

Table 22. Size Field versus AGP Memory Allocation

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Memory Allocated
1	1	1	1	1	1	1	32 Mbytes
1	1	1	1	1	1	0	64 Mbytes
1	1	1	1	1	0	0	128 Mbytes
1	1	1	1	0	0	0	256 Mbytes
1	1	1	0	0	0	0	512 Mbytes
1	1	0	0	0	0	0	1 Gbytes
1	0	0	0	0	0	0	2 Gbytes

Bits 24–4 Base Address Low (always reads 0)—This field are cleared to indicate that the minimum allocated memory size is 32 Mbytes.

Bit 3 Prefetchable (always reads 1)—This bit is set to indicate that the graphics memory area can be prefetched.

Bits 2–1 Type (always reads 0)—These bits are cleared to indicate that this base register is 32 bits wide and mapping can be performed anywhere in the 32-bit address space.

Bit 0 Memory (always reads 0)—This bit is cleared to indicate that this base address register maps into memory space.

Base Address Register 1 (BAR1) Device 0 Offset 17h–14h

	Bits 31–12																			Bits 11–4								Bit 3	Bits 2–1		Bit 0
	Base Address High																			Base Address Low								Pre	Type		Mem
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

This register is used by the AGP driver software to set the memory location of the AGP memory-mapped control registers.

Bits 31–12 Base Address High (RW) (default = 000000h)—This field is loaded by BIOS firmware to determine the base address A[30:11] of the memory-mapped AGP registers (BAR1). See page 173 for more information.

Bits 11–4 Base Address Low (always reads 0)—This field is cleared to indicate that 4 Kbytes is allocated to AGP memory-mapped control registers and that the registers reside in a 4-Kbyte boundary per the *PCI Local Bus Specification, Revision 2.2*.

Bit 3 Prefetchable (always reads 1)—This bit is set to indicate that this range can be prefetched.

Bits 2–1 Type (always reads 0)—These bits are cleared to indicate that BAR1 is 32 bits wide and mapping can be performed anywhere in the 32-bit address space.

Bit 0 Memory (always reads 0)—This bit is cleared to indicate that BAR0 maps into memory space.

Base Address Register 2 (BAR2) Device 0 Offset 1Bh–18h

	Bits 31–24								Bits 23–2																				1	0
	Reserved								PM2_Block Base Address [31:10]																				R	I/O
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits 31–24 Reserved (always reads 0)

Bits 23–2 PM2 Block Base Address (RW)—This field contains the base address of the power management register block. This field forms the upper part of BAR2 containing A[31:10]. This field is loaded by BIOS firmware and specifies the base of the PM2_BLK.

Bit 1 Reserved (always reads 0)

Bit 0 I/O space (always reads 1)—This bit indicates that the base address register maps to x86 I/O space.

Capabilities Pointer — Device 0 Offset 37h–34h

Bits 31–8	Bits 7–0
Reserved	CAP_PTR
Reset 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 0 1 0 0 0 0 0

Bits 31–8 Reserved (always reads 0)

Bits 7–0 CAP_PTR (always reads A0h)—This field contains the PCI device 1 offset of the configuration register group in the AMD-751 system controller specifically reserved for AGP functions. This register group is the first item in the *New Capabilities* mechanism described in an amendment to the *PCI Local Bus Specification, Revision 2.1*.

Base Address Chip Select Register 0 — Device 0 Offset 41h–40h

Bits 15–7	Bits 6–1	0
Bank 0 Base Address A[31:23]	Bank 0 address Mask A[28:23]	EN
Reset 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0	0

Bits 15–7 Bank 0 Base Address A[31:23] (RW)— These bits determine the base or start address of the bank 0 chip select. The bank 0 address mask bits determine which of the address bits are to be used by the compare logic to generate a chip select, depending on the size of the memory bank.

Note: *Logically, chip select programming would be described in the following way: (Mem_CS[n] = true) if (A[31:23] AND (NOT Bank(n) Mask)) = (Bank(n) Base AND (NOT Bank(n) Mask)).*

Bits 6–1 Bank 0 Address Mask A[28:23] (RW)—These bits are ANDed with A[28:23] from the processor to determine the size of the memory bank (8 Mbytes, 16 Mbytes, etc.).

Note: *The minimum bank size supported is 8 MByte.*

Bit 0 Bank 0 Enable (RW)

0 = Memory bank is disabled (default)
1 = Memory bank enabled

Note: *BIOS firmware must configure the largest banks first as the lowest addressed memory, then increasing addresses with decreasing bank sizes available.*

Base Address Chip Select Register 1 — Device 0 Offset 43h–42h

	Bits 15–7									Bits 6–1						0
	Bank 1 Base Address A[31:23]									Bank 1 Address Mask A[28:23]						EN
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15–7 **Bank 1 Base Address A[31:23] (RW)**—See Base Address Chip Select Register 0 on page 137.

Bits 6–1 **Bank 1 Address Mask A[28:23] (RW)**—See Base Address Chip Select Register 0.

Bit 0 **Bank 1 Enable (RW)**

0 = Memory bank is disabled (default)
1 = Memory bank enabled.

Base Address Chip Select Register 2 — Device 0 Offset 45h–44h

	Bits 15–7									Bits 6–1						0
	Bank 2 Base Address A[31:23]									Bank 2 Address Mask A[28:23]						EN
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15–7 **Bank 2 Base Address A[31:23] (RW)**—See Base Address Chip Select Register 0 on page 137.

Bits 6–1 **Bank 2 Address Mask A[28:23] (RW)**—See Base Address Chip Select Register 0.

Bit 0 **Bank 2 Enable (RW)**

0 = Memory bank is disabled (default)
1 = Memory bank enabled

Base Address Chip Select Register 3 — Device 0 Offset 47h–46h

	Bits 15–7									Bits 6–1						0
	Bank 3 Base Address A[31:23]									Bank 3 Address Mask A[28:23]						EN
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15–7 **Bank 3 Base Address A[31:23] (RW)**—See Base Address Chip Select Register 0 on page 137.

Bits 6–1 **Bank 3 Address Mask A[28:23] (RW)**—See Base Address Chip Select Register 0.

Bit 0 **Bank 3 Enable (RW)**

0 = Memory bank is disabled (default)
1 = Memory bank enabled

Base Address Chip Select Register 4 Device 0 Offset 49h–48h

	Bits 15–7									Bits 6–1						0
	Bank 4 Base Address A[31:23]									Bank 4 Address Mask A[28:23]						EN
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15–7 **Bank 4 Base Address A[31:23] (RW)**—See Base Address Chip Select Register 0 on page 137.

Bits 6–1 **Bank 4 Address Mask A[28:23] (RW)**—See Base Address Chip Select Register 0.

Bit 0 **Bank 4 Enable (RW)**

0 = Memory bank is disabled (default)
1 = Memory bank enabled

Base Address Chip Select Register 5 Device 0 Offset 4Bh–4Ah

	Bits 15–7									Bits 6–1						0
	Bank 5 Base Address A[31:23]									Bank 5 Address Mask A[28:23]						EN
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15–7 **Bank 5 Base Address A[31:23] (RW)**—See Base Address Chip Select Register 0 on page 137.

Bits 6–1 **Bank 5 Address Mask A[28:23] (RW)**—See Base Address Chip Select Register 0.

Bit 0 **Bank 5 Enable (RW)**

0 = Memory bank is disabled (default)
1 = Memory bank enabled

SDRAM Address Mapping Control Register 1/0 — Device 0 Offset 50h

	Bit 7	6	5	4	3	2	1	Bit 0
	Reserved	Address Mode 1	#Banks 1	Reserved		Address Mode 0	#Banks 0	Reserved
Reset	0	0	0	0	0	0	0	0

Bit 7 **Reserved (always reads 0)**

Bits 6 **CS1 Address Mode (RW)**—This bit specifies the row and column addressing as shown in Table 23 on page 142.

Bit 5 **Number of Banks in CS1 (RW)**—This bit specifies the number of internal DRAM banks in this chip select.

0 = Two banks (default)
1 = Four banks

Bit 4–3 **Reserved (always reads 0)**

Bit 2 **CS0 Address Mode (RW)**—This bit specifies the row and column addressing as shown in Table 23 on page 142.

Bit 1 **Number of Banks in CS0 (RW)**—This bit specifies the number of internal DRAM banks in this chip select.

0 = Two banks (default)
1 = Four banks

Bit 0 **Reserved (always reads 0)**

SDRAM Address Mapping Control Register 3/2 — Device 0 Offset 51h

	Bit 7	6	5	4	3	2	1	Bit 0
	Reserved	Address Mode 3	#Banks 3	Reserved		Address Mode 2	#Banks 2	Reserved
Reset	0	0	0	0	0	0	0	0

Bit 7 **Reserved (always reads 0)**

Bit 6 **CS3 Address Mode (RW)**—This bit specifies the row and column addressing as shown in Table 23 on page 142.

Bit 5 **Number of Banks in CS3 (RW)**—This bit specifies the number of internal DRAM banks in this chip select.

0 = Two banks (default)
1 = Four banks

Bit 4–3 **Reserved (always reads 0)**

Bit 2 **CS2 Address Mode (RW)**—This bit specifies the row and column addressing as shown in Table 23 on page 142.

Bit 1 **Number of Banks in CS2 (RW)**—This bit specifies the number of internal DRAM banks in this chip select.

0 = Two banks (default)
1 = Four banks

Bit 0 **Reserved (always reads 0)**

SDRAM Address Mapping Control Register 5/4 — Device 0 Offset 52h

	Bit 7	6	5	4	3	2	1	Bit 0
	Reserved	Address Mode 5	#Banks 5	Reserved		Address Mode 4	#Banks 4	Reserved
Reset	0	0	0	0	0	0	0	0

Bit 7 **Reserved (always reads 0)**

Bit 6 **CS5 Address Mode (RW)**—This bit specifies the row and column addressing as shown in Table 23 on page 142.

Bit 5 **Number of Banks in CS5 (RW)**—This bit specifies the number of internal DRAM banks in this chip select.

0 = Two banks (default)
1 = Four banks

Bit 4–3 **Reserved (always reads 0)**

Bit 2 **CS4 Address Mode (RW)**—This bit specifies the row and column addressing as shown in Table 23 on page 142.

Bit 1 **Number of Banks in CS4 (RW)**—This bit specifies the number of internal DRAM banks in this chip select.

0 = Two banks (default)
1 = Four banks

Bit 0 **Reserved (always reads 0)**

Table 23. Mapping Processor Address Lines to Memory Address Lines

		SDRAM													
Reg 50h Addr Mode		**MA14**	**MA13**	**MA12**	**MA11**	**MA10**	**MA9**	**MA8**	**MA7**	**MA6**	**MA5**	**MA4**	**MA3**	**MA2**	**MA1**	**MA0**	**Row:Col**
0 16 Mbit	Row Column		11 11			12 PC	22 24	21 23	20 10	19 9	18 8	17 7	16 6	15 5	14 4	13 3	x4 (11:10) x8 (11:9) x16 (11:8)
1 64 Mbit 128 Mbit	Row Column	12 12	11 11	12	24 27	23 PC	22 26	21 25	20 10	19 9	18 8	17 7	16 6	15 5	14 4	13 3	x4 (14:11) x8 (14:10) x16 (14:9) x32 (14:8)

Mode 0, 2 Bank: MA13 = Bank select

Mode 1, 2 Bank: MA13 = Bank select

Mode 1, 4 Bank: MA[13:12] = Bank select

DRAM Timing Register — Device 0 Offset 55h–54h

	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
	PHL		ICL[1:0]		TRC			TRP		TRAS			TCL		TRCD	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15–14 PH Limit (RW)—These bits specify the number of consecutive page-hit requests to allow before choosing a non-page-hit request.

00 = 1 cycle(default)
01 = 4 cycles
10 = 32 cycles (recommended safe configuration)
11 = 64 cycles

Bits 13–12 Idle Cycle Limit [1:0] (RW)—These bits specify the number of idle cycles to wait before precharging an idle bank. (Idle cycles are defined as cycles where no valid request is asserted to the MCT.)

Idle Cyle Limit[2:0]*

000 = 0 cycle (default)
001 = 8 cycles (recommended safe configuration)
010 = 12 cycles
011 = 16 cycles
100 = 24 cycles
101 = 32 cycles
110 = 48 cycles
111 = Disable idle precharge

* See Idle Cyle Limit [2] on page 144.

Bits 11–9 TRC Bank Cycle Time Value (RW)—These bits specify the minimum time from activate to activate of the same bank.

000 = 3 cycles (default)
001 = 4 cycles
010 = 5 cycles
011 = 6 cycles
100 = 7 cycles
101 = 8 cycles (recommended safe configuration)
110 = Reserved
111 = Reserved

Bits 8–7 TRP SRAS Precharge (RW)—These bits specify the delay from precharge command to activate command.

00 = 3 cycle (default) (recommended safe configuration)
01 = 2 cycles
1x = 1 cycles

Bits 6–4 **TRAS Value (RW)**—These bits specify the minimum bank (SRAS[2:0]#) active time.

000 = 2 cycles (default)
001 = 3 cycles
010 = 4 cycles
011 = 5 cycles
100 = 6 cycles
101 = 7 cycles (recommended safe configuration)
110 = Reserved
111 = Reserved

Bits 3–2 **TCL SDRAM SCAS Latency Value (RW)**—These bits specify the delay from SCAS[2:0]# to data valid.

00 = 3 cycle (default) (recommended safe configuration)
01 = 2 cycles
10 = Reserved
11 = 4 cycles

Bits 1–0 **TRCD SRAS to SCAS Latency Value (RW)**—These bits specify the delay from the activation of a bank to the time that a read or write command is accepted.

00 = 1 cycle (default)
01 = 2 cycles
10 = 3 cycles (recommended safe configuration)
11 = 4 cycles

DRAM CS Driver Strength Register — Device 0 Offset 57h–56h

	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
	Reserved							ICL[2]	Address Bus B DRV		Address Bus A DRV		Controls DRV		DQM DRV	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15–9 **Reserved (always reads 0)**

Bit 8 **Idle Cycle Limit [2] (RW)**—This bit, along with those described on page 143, specify the number of idle cycles to wait before precharging an idle bank.

Bits 7–6 **SDRAM Address Bus B and ClkOut DRV (RW)**—This bit specifies driver strength selection for the SDRAM MAdB and clock signals.

00 = Light Load—One single-sided DIMM
01 = Medium Light Load—Not used
10 = Medium Heavy Load—Two single-sided DIMMs or one double-sided DIMM
11 = Heavy Load—Two double-sided DIMMs

Bits 5–4 **SDRAM Address Bus A DRV (RW)**—This bit specifies driver strength selection for the SDRAM MAdA signals.

00 = Light Load—One single-sided DIMM
01 = Medium Light Load—Not used
10 = Medium Heavy Load—Two single-sided DIMMs or one double-sided DIMM
11 = Heavy Load—Two double-sided DIMMs

Bits 3–2 **SDRAM Controls DRV (RW)**—These bits specify driver strength selections for SRAS[2:0]#, SCAS[2:0]#, MCKE[2:0], CS[5:0]#, and WE[2:0]# signals.

00 = Drive strength selected Low
01 = Drive strength selected Medium Low (Recommended setting)
10 = Drive strength selected Medium High
11 = Drive strength selected High

Bits 1–0 **SDRAM DQM Bus DRV (RW)**—This bit specifies driver strength selection for the SDRAM DQM signals.

00 = Drive strength selected Low
01 = Drive strength selected Medium Low (Recommended setting)
10 = Drive strength selected Medium High
11 = Drive strength selected High

DRAM ECC Status Register — Device 0 Offset 59h–58h

	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
	Reserved						ECC Status		Reserved		Failing ECC Chip Select					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15–10 **Reserved (always reads 0)**

Bits 9–8 **ECC Status (RW)**—This field indicates the status of the DRAM error correcting code detect logic. An I/O write must clear both bits in this field before any new status can be recorded.

00 = No error (default)
01 = Multiple bit error detected (SERR# asserts)
10 = Single bit error detected
11 = Single and multiple bit error detected (SERR# asserts)

Bits 7–6 **Reserved (always reads 0)**

Bits 5–0 **ECC CS Status (RO)**—This field indicates the chip select where the ECC error occured. Bit 0 indicates CS0, bit 1 indicates CS1, etc.

DRAM Mode/Status Register — Device 0 Offset 5Bh–5Ah

	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
	Reserved						SD Init	Type	MWE	Reserved		BRE	R	EN	Cycles	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15–10 Reserved (always reads 0)

Bit 9 SDRAM Init (RWS)—This bit is used to start the SDRAM initialization sequence. When set, this bit cannot be reset. BIOS code should first set SDRAM timing parameters and signal drive strength prior to initiating this bit.

Bit 8 SDRAM Type (RW0)

0 = SDRAM (default)
1 = ESDRAM (not supported by the AMD-751 system controller)

Bit 7 Mode Write Enable (RW)—This bit is used by the BIOS to set the DRAM mode register. TCL and Large Burst Enable must be set before this bit is asserted (see page 144). The MCT clears this bit when the mode register write is complete.

0 = Write to DRAM mode register is disabled/done (default)
1 = Mode register write enabled

Bits 6–5 Reserved (always reads 0)

Bit 4 Burst Refresh Enable (RW)

0 = Refresh requests are only queued if memory requests are currently being serviced (default)
1 = Up to four refresh requests are queued before being sent to the MCT

Bit 3 Large Burst Enable (always reads 0)

0 = Eight quadword burst (default)
1 = Four quadword burst

Bit 2 ECC Enable (RW)

0 = ECC disabled (default)
1 = ECC enabled

Bits 1–0 Cycles per Refresh (RW)—This field specifies the number of 100-MHz clock cycles between refresh request.

00 = 2048 cycles between refresh (default)
01 = 1536 cycles between refresh (recommended)
10 = 1024 cycles between refresh
11 = 512 cycles between refresh

BIU Control and Status Register — Device 0 Offset 63h–60h

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Probe Enable	Reserved R/W			XCA Probe Count			XCA Read Count			XCA Write Count			Halt DSCEna	SGDis Ena	Probe Limit
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
	Probe Limit		Ack Limit				Bypass Enable	DCOut Delay		DCin Delay				WR2R D Dly	RD2WR Delay	
Reset	0	0	0	0	1	1	0	X	X	X	X	X	X	X	X	X

Bit 31 **Probe Enable (RW)**—When set, this bit allows probes to be sent to the processor.

Bits 30–28 **Reserved (always RW0)**—This field must always be written as 000 for maximum performance.

Bits 27–25 **XCA Probe Count (RW)**—This field is set by the BIOS firmware with the maximum number of consecutive AMD Athlon system bus grants for Probe transfers allowed before the AMD-751 system controller forces another type of transfer to gain access to the AMD Athlon system bus. The count limit prevents one type of transfer from dominating the AMD Athlon system bus. The recommended value is 010b.

Bits 24–22 **XCA Read Count (RW)**—This field is set by the BIOS firmware with the maximum number of consecutive AMD Athlon system bus grants for Read transfers allowed before the AMD-751 forces another type of transfer to gain access to the AMD Athlon system bus. The count limit prevents one type of transfer from dominating the AMD Athlon system bus. The recommended value is 110b.

Bits 21–19 **XCA Write Count (RW)**—This field is set by the BIOS firmware with the maximum number of consecutive AMD Athlon system bus grants for Write transfers allowed before the AMD-751 forces another type of transfer to gain access to the AMD Athlon system bus. The count limit prevents one type of transfer from dominating the AMD Athlon system bus. The recommended value is 100b.

Bit 18 **Halt Disconnect Enable (RW)**

0 = No disconnect after a Halt special cycle (default)
1 = Disconnect after a Halt special cycle

Note: *See ACPI Power States on page 108 for more information.*

Bit 17 **Stop Grant Disconnect Enable (RW)**

0 = No disconnect after a Stop Grant special cycle (default)
1 = Disconnect after a Stop Grant special cycle

Bits 16–14 **Probe Limit (RW)**—This field is set by the BIOS firmware with the maximum probes that the processor can handle.

000 = 1 probe (default)
001 = 2 probes
010 = 3 probes
.
.
111 = 8 probes

Bits 13–10 **Ack Limit (RO)**—BIOS firmware reads this field to determine how many outstanding 'un-acked' AMD Athlon system bus commands can be sent to the AMD-751 system controller.

0000= 1 un-acked commands
0001= 2 un-acked commands
0010= 3 un-acked commands
0011= 4 un-acked commands (default)
.
.
.
1111= 16 un-acked commands

Bit 9 **Bypass Mode Enable (RW)**—When set, the AMD-751 allows low-latency accesses to memory. The low-latency access "bypasses" internal FIFOs and arbiters when no PCI or APCI operations are pending. This mode is valid for use in AMD Athlon processor systems only.

Note: *Bypass mode is available in Revision C and later of the AMD-751 system controller. In previous revisions, this bit was used as the RIH enable control. RIH probes are always disabled.*

Bits 8–7 **DC Out Delay (RO)**—This field specifies the number of system (normally 100-MHz) clock cycles from a processor read command and the start of data.

00 = Reserved
01 = 1 cycles
10 = 2 cycles
11 = 3 cycles

Bits 6–3 **DC in Delay (RO)**—This field specifies the number of system (100-MHz) clocks from a processor write command and the start of data.

0000= 1 clock
0001= 2 clocks
.
.
.
1111= 16 clocks

Bit 2 **WR2RD Delay (RO)**—This field specifies the number of AMD Athlon system bus cycles that are inserted between write and read transfers to allow the data bus to turn around

Bits 1–0 **RD2WR Delay (RO)**—This field specifies the number of AMD Athlon system bus cycles that are inserted between read and write transfers to allow the data bus to turn around.

BIU SIP Register — Device 0 Offset 67h–64h

	Bit 31	Bits 30–29	Bits 28–27	Bits 26–0
	Clock FO	Data Init Cnt	Addr Init Cnt	SIP Packet
Reset	0	INIT Logic		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Bit 31 **Clock Forward Offset (RW)**—This affects the clock forwarded data bus timing:

0 = AMD-751 system controller delays the assertion of SDATA [31:16] and [63:48] bits and appropriate clocks by approximately 1000ps.
1 = All data groups are forwarded at the same time (nominally aligned with a system clock edge)

Bits 30–29 **Data FIFO Initialize Count (RO)**—This field displays the value loaded by the initialization logic in the data receive FIFO counters.

Bits 28–27 **Address FIFO Initialize Count (RO)**—This field displays the value loaded by the initialization logic in the address receive FIFO counters.

Bits 26–0 **SIP[27:1] Serial Initialization Packet (RO)**—This field contains the values loaded into the processor during the AMD Athlon system bus connect protocol. The initial state depends on the initialization logic.

BIU 1 Status Register — Device 0 Offset 69h–68h

	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
	Reserved															
Reset	0	0	X	X	0	0	0	0	0	0	0	0	X	X	X	0

Bits 15–0 **Reserved**—Reserved for dual processor implementation.

MRO Control Register — Device 0 Offset 71h–70h

	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
	Reserved					PCIPipe Enable	PCIBlk WrFEn	Reserved			Memory Request Disable				MWD	RD
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit s 15–11 **Reserved (always reads 0)**

Bit 10 **PCI Pipeline Enable (RW)**—This bit should be set to 1 for optimal operation. When clear, all PCI tranfers are checked against outstanding processor read probes. Those tranfers with matching block addresses are then stalled until the matching read probe is complete. When set, PCI transfers are pipelined for highest performance.

Bit 9 **PCI Block Write Fast Enable (RW)**—This bit should be set to 1 for optimal operation. When set, the AMD-751 system controller sends an NOP invalidate probe to the AMD Athlon processor for PCI block writes and allows the PCI block write to memory to continue. When clear, the AMD-751 sends a Read-if-Dirty invalidate probe to the processor and waits for the data to return from the processor cache before allowing the PCI block write to memory.

Bit s 8–6 **Reserved (RW0)**—These bits must remain 0 for proper operation.

Bit s 5–2 **Memory Request Disable (RW)**—These bits are for testing purposes only. When set, these bits disable request entries in the memory read queue (MRQ) (default 000).

Bit 1 **Memory Write Queue Disable (RW)**—This bit is for testing purposes only.

0 = Enables the request entry in the memory write queue (MWQ) (default)
1 = Disables the request entry in the MWQ

Bit 0 **Reorder Disable (RW)**

0 = The memory request organizer (MRO) reorders memory requests to optimize memory performance
1 = The MRO does not reorder memory requests (default)

Who Am I (WHAMI) Register — Device 0 Offset 81h–80h

	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
	First AMD Athlon™ System Bus ID								WHAMI							
Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bits 15–8 **First AMD Athlon™ System Bus ID (RO)**—This field contains the ID of the first processor to read this register.

Bits 7–0 **Who Am I (RO)**—This field returns the ID of the processor that accesses it.

PCI Arbitration Control Register — Device 0 Offset 84h–85h

	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
	MDA Suprt	PCIW pRtr	APCI WpRtr	DisRD err	DisAP CIeP	DisPCI eP	AGPA D	SBlkDi s	PMRe gEna	15Mh ole	14Mh ole	EV6	TLTD	APE	PPE	Park
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 15 **MDA Support (RW)**—This bit allows monchrome display adapters (MDA) to be used simultaneously with AGP display cards. Use this bit in conjunction with the VGA enable bit (see page 171) as follows:

VGA = 0, MDA = 0—All VGA and MDA references go to the PCI bus
VGA = 0, MDA = 1—Undefined
VGA = 1, MDA = 0—MDA only operations (I/O 3BFh) go to PCI, all other graphics references to AGP
VGA = 1, MDA = 1—All MDA references go to PCI and all AGP references go to AGP

MDA address ranges are defined as follows:

Memory—0B0000h–0B7FFFh
I/O—3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh

Bit 14 **PCI Write-Post Retry (RW)**—When set, this bit enables retries on the PCI if there are pending posted writes.

Bit 13 **APCI Write-Post Retry (RW)**—When set, this bit enables retries on the APCI if there are pending posted writes.

Bit 12 **Disable Read Data Error (RW)**—When set, this bit disables the AMD-751 system controller from reporting a data read error to the processor if the BUI cycle was aborted. Instead, the AMD-751 then returns a data value of all bits equal to 1b.

Bit 11 **Disable APCI Early Probe (RW)**—When set, this bit disables the AMD-751 system controller from issuing an early cache snoop to the processor when an APCI (AGP bus) master requests a memory write cycle. In the default mode, as soon as the AMD-751 detects a memory write cycle from an external APCI master, it sends a probe only request to the MRO, which results in a processor snoop.

Bit 10 **Disable PCI Early Probe (RW)**—This bit works exactly the same as bit 11, except that it affects PCI master requests rather than APCI requests.

Bit 9 **AGP Arbiter Pipelining Disable (RW)**—This bit disables the AGP arbiter from pipelining grants onto the bus.

0 = Enabled (default)
1 = Disable the AGP arbiter from pipelining grants onto the bus

Bit 8 **SB Lock Disable (RW)**—This bit controls the response of the AMD-751 system controller to a PCI request by the AMD-756 peripheral bus controller.

0 = The AMD-751 ensures that all previous requests from the BIU and PCI are flushed out before granting the AMD-756 the PCI bus
1 = Disable the flushing of previous requests

Bit 7 **Power Management Register Access Enable (RW)**—This bit controls reading and writing to the power management register (BAR2).

0 = Accesses to the power management register address (BAR2) are forwarded to the PCI bus, which results in a PCI master abort cycle (default)
1 = Enable access to the power management register

Bit 6 **15Mbyte Hole Enable (RW)**—When set, this bit creates a 'hole' in memory from 15 Mbytes to 16 Mbytes, and the PCI decode logic does not assert a match for those addresses.

Bit 5 **14Mbyte Hole Enable (RW)**—When set, this bit creates a 'hole' in memory from 14 Mbytes to 15 Mbytes, and the PCI decode logic does not assert a match for those addresses.

Bit 4 **EV6 Mode (RW)**—When set, this bit indicates that the PCI interface decodes memory hits in the EV6 mode. There are no memory holes and DMA can be performed on any address that lies within the SDRAM map.

0 = x86 mode (default)
1 = EV6 mode

Bit 3 **Target Latency Timer Disable (RW)**—When the AMD-751 system controller acts as a PCI target, it has a latency timer that retries the write cycle if its buffers are full for more than 8 bus clocks (16 clocks for the first transfer).

0 = Enabled (default)
1 = Disable the target latency timer on both the standard PCI and AGP PCI interfaces

Bit 2 **APCI Prefetch Enable (RW)**—This bit enables the AMD-751 system controller to prefetch data from the SDRAM when a PCI master on the AGP bus reads from the main memory.

0 = Prefetch disabled (default)
1 = Prefetch enabled

Bit 1 **PCI Prefetch Enable (RW)**—This bit enables the AMD-751 to prefetch data from the SDRAM when a PCI master on the standard PCI bus reads from the main memory.

0 = Prefetch disabled (default)
1 = Prefetch enabled

Bit 0 **Park PCI (RW)**—This bit controls where the arbiter defaults to when there is no request pending. Sometimes this is referred to as processor-centric (parking on the processor) or memory-centric. Generally, a processor-centric system has improved processor benchmarks and a memory-centric system has improved overall system performance. The philosophy in a memory-centric system is that the last requestor is most likely to be the next requestor.

0 = The arbiter parks on the processor only (default)
1 = Enable parking for the PCI master (recommended)

PCI and APCI Chaining Register — Device 0 Offset 86h

	Bit 7	6	5	4	3	2	1	Bit 0
	Reserved						Chaining Enable	
Reset	0	0	0	0	0	0	0	0

Bit 1 **Enable APCI Chaining**—This bit allows chaining of back-to-back write operations to APCI (from the processor). Only sequencially-addressed write transactions that do not cross 4-Kbyte page boundaries can be combined into one bus burst transfer (chaining).

Bit 0 **Enable PCI Chaining**—This bit allows chaining of back-to-back write operations to PCI (from the processor). Only sequencially-addressed write transactions that do not cross 4-Kbyte page boundaries can be combined into one bus burst transfer (chaining).

Note: *Enable APCI chaining and enable PCI chaining bits are available on the AMD-751 system controller Revision C and later. In previous revisions, these bits are read-only and always read 0.*

AGP VGA BIOS Mask Register — Device 0 Offset 87h

	Bit 7	6	5	4	3	2	1	Bit 0
	DC	D8	D4	D0	CC	C8	C4	C0
Reset	0	0	0	0	0	0	0	0

Bits 15–8 **AGP VGA BIOS Address (RW)**—This field indicates the corresponding 16-Kbyte segment or segments that contains the VGA BIOS on the AGP bus. The range of bit settings are as follows:

Bit 0 = address range 0xC0000h–0xC3FFFh
Bit 1 = address range 0xC4000h–0xC7FFFh
Bit 3 = address range 0xC8000h–0xCBFFFh
Bit 4 = address range 0xCC000h–0xCFFFFh
Bit 5 = address range 0xD0000h–0xD3FFFh
Bit 6 = address range 0xD4000h–0xD7FFFh
Bit 7 = address range 0xD8000h–0xDBFFFh
Bit 8 = address range 0xDC000h–0xDFFFFh

Each RW bit determines if accesses in the respective address range are forwarded from the primary to the secondary PCI bus. When set, these bits indicate that the corresponding segment (16 Kbytes) should be mapped to the AGP PCI (secondary) bus. One or more of these bits should be set if the AGP graphics card has a BIOS.

0 = Do not forward (default)
1 = Forward

Bits 7–2 **Reserved (always reads 0)**

Config Status#1 Device 0 Offset 89h–88h

	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
	Reserved				Reserved				Reserved				Processor Divider			
Reset	0	0	0	0	SBA7	SBA6	SBA5	SBA4	0	0	0	0	SBA3	SBA2	SBA1	SBA0

Bits 15–12 Reserved (always reads 0)

Bits 11–8 Reserved for Dual Processor Implementation

Bits 7–4 Reserved (always reads 0)

Bits 3–0 Processor Divider (RO)—This field contains the processor divider field supplied by the AMD Athlon system bus. Together with the CLK speed and the bus length fields, this field allows the AMD-751 system controller to properly program the AMD Athlon processor interface logic using the SIP protocol. The default value comes from bus pins AD[3:0].

Config Status #2 Device 0 Offset 8Bh–8Ah

	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
	Reserved							ProcB Trshld	AGP/CoreCLK Ratio		CoreCLK		Reserved		length 0	
Reset	0	0	0	0	0	0	0	AD40	0	PLLDv	AD31	AD30	X	X	AD11	AD10

Bits 15–9 Reserved (always reads 0)

Bit 8 Processor Bus Threshhold (RO)—This bit indicates the threshold range for the AMD Athlon system bus I/O cells.

0 = Low threshold of between 1.35V to 1.9V
1 = High threshold of between 2.0V to 2.2V

Bits 7–6 AGP to Core Clock Ratio (RO)—This field indicates the ratio of the AGP logic clock and the system clock used to run the BIU and memory control logic. Bit 6 is controlled by the PLL divisor pin. Bit 7 is hard wired to 0.

00 = AGP clock to system clock ratio of 1.0 to 1.0
01 = AGP clock to system clock ratio of 1.0 to 1.5 (production setting)
1x = Reserved

Bits 5–4 Clock Speed (RO)—The default comes from the bus pins AD[31:30]. This field defines the speed of the system clock received by the AMD-751 system controller.

00 = System clock speed is 100 MHz (production setting)
01 = System clock speed is 66 MHz
10 = System clock speed is 90 MHz
11 = Reserved

Bits 3–2 Reserved for Dual Processor Implementation

Bits 1–0 AMD Athlon™ System Bus Length (RO)—This field indicates the relative length of the AMD Athlon system bus trace routing on the motherboard. The default comes from bus pins AD[11:10].

00 = Short, non-AMD Athlon system bus design
01 = Single AMD Athlon system bus slot, close
10 = Far AMD Athlon system bus slot, used for dual processor configurations
11 = Farthest length AMD Athlon system bus slot (dual processor designs)

AGP Capability Identifier — Device 0 Offset A3h–A0h

	Bits 31–24								Bits 23–20				19	18	17	16	Bits 15–8								7	6	5	4	3	2	1	0
	Reserved								Major Revision				Minor Revision				Next Pointer								Capabilities Identifier							
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits 31–24 Reserved (always reads 0)

Bits 23–20 Major Revision of AGP Specification (RO)—These bits indicate the AGP-specification major revision to which the device conforms.

0000 = Revision 0
0001 = Revision 1
0010 = Revision 2

Note: *See Bits 19–16 for an example.*

Bits 19–16 Minor Revision of AGP Specification (RO)—These bits indicate the AGP-specification minor revision to which the device conforms.

0000 = Revision x.0
0001 = Revision x.1
0010 = Revision x.2

For example, if bits 23–16 = 20h, the device conforms to AGP-specification revision 2.0.

Bit 15–8 Next Pointer (always reads 0)—The pointer to the next item in the new capabilities linked list is set to null to indicate the last item in the list.

Bits 7–0 Capability Identifier (always reads 02h)—The default value 02h indicates AGP as assigned by the PCI Special Interest Group.

AGP Status — Device 0 Offset A7h–A4h

31	30	29	28	27	26	25	24	Bits 23–10	Bit 9	Bits 8–6	5	Bits 4–2	Bits 1–0
Maximum Request Depth								Reserved	SBAE	Reserved	4G	Reserved	TRC
Reset 0	0	0	0	1	1	1	1	0 0 0 0 0 0 0 0 0 0	1	0 0 0	0	0 0 0	1 1

Bits 31–24 Maximum Request Depth (always reads 0Fh)—The read-only value of 0Fh indicates that the AMD-751 system controller can handle a maximum of 16 AGP requests.

Bits 23–10 Reserved (always reads 0)

Bit 9 Sideband Address (always reads 1)—This bit is set to indicate that the AMD-751 supports sideband addressing.

Bits 8–6 Reserved (always reads 0)

Bit 5 4-Gigabyte Address Space (RO)—This bit reflects the setting of the Command Register, Offset A8h–ABh, bit 5.

0 = Address space is limited to four Gbytes (default)
1 = Address space can be greater than four Gbytes

Bits 4–2 Reserved (always reads 0)

Bits 1–0 Transfer Rate Capability (always reads 11b)—This field indicates that the AMD-751 supports both 1x and 2x data transfers.

AGP Command Register #2 — Device 0 Offset ABh–A8h

	Bits 31–10	Bit 9	Bit 8	Bits 7–6	5	Bits 4–2	Bits 1–0
	Reserved	SBAE	AGPE	Reserved	4G	Reserved	TRS
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0 0	0	0 0 0	0 0

Bits 31–10 Reserved (always reads 0)

Bit 9 Sideband Address Enable (RW)

0 = SBA operations are disabled (default)
1 = SBA operations are enabled

Bit 8 AGP Enable (RW)

0 = AGP operations are ignored (default)
1 = AGP operations are accepted

Bits 7–6 Reserved (always reads 0)

Bit 5 4G_ENA (always reads 0)—When this bit is 0, it indicates the address range is up to four Gbytes. The AMD-751 system controller only supports 32-bit addressing.

Bits 4–2 Reserved (always reads 0)

Bits 1–0 Transfer Rate Select (RW)—One bit must be set in this field and the other cleared to indicate the desired AGP data transfer rate.

00 = Reset condition (default)
01 = Selects 1x transfer mode
10 = Selects 2x transfer mode
11 = Not allowed

AGP Virtual Address Space — Device 0 Offset AF–ACh

	Bits 31 – 17	16	Bits 15– 4	3	2	1	0
Reset	Reserved	VI	Reserved	VAS			GE
	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1	0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0

Bits 31–17 Reserved (always reads 0)

Bit 16 VGA ISA Address Space (RW)

0 = Address bits A[15:10] are used for decoding
1 = Address bits A[9:0] are used for decoding (default)

Bits 15–4 Reserved (always reads 0)

Bits 3–1 **Virtual Address Space (RW)**—This field defines the amount of virtual address space (VAS) allocated to the GART by the system BIOS. During its memory mapping routine, the BIOS reads the graphics controller to determine the amount of graphics memory required and adjusts these bits accordingly. Changing these bits automatically changes Device 0, Offset 10h, bits 30–25 (see page 135).

The operating system allocates the actual number of non-contiguous 4-Kbyte blocks of physical system memory allocated to the GART. The total amount of allocated physical memory can never exceed the VAS size.

000 = 32 Mbytes virtual address space (default)
001 = 64 Mbytes
010 = 128 Mbytes
011 = 256 Mbytes
100 = 512 Mbytes
101 = 1 Gbytes
110 = 2 Gbytes

Bit 0 **GART Enable (RW)**—This bit determines whether or not the system BIOS allocates virtual address space for the GART. If the Processor-to-PCI bridge (Device 0, Offset 10h) BAR0 is set to 0, no memory is allocated. The PCI-to-PCI bridge (Device 1) capabilities pointer is set to point to the next item in the linked list, or null if there is no other item. This bit is set by the BIOS PCI enumeration routines. System BIOS allocates virtual address space for the GART based upon the value in bits [3:1].

0 = GART operations are not valid (default)
1 = GART operations are valid

AGP Mode Control Register #1 — Device 0 Offset B0h

	7	Bits 6–0						
	SynEn	Reserved						
Reset	0	0	0	0	0	0	0	0

Bit 7 **Sync Enable (RW)**

0 = No synchronization is guaranteed (default)
1 = The AMD-751 system controller enables all writes to the GART range from processor to memory to be completed before initiating processor-to-AGP cycles, allowing synchronization between the processor and AGP

Bits 6–0 **Reserved (RW0)**—These bits must remain 0 for proper operation.

AGP Mode Control Register #2 — Device 0 Offset B2h

	7	6	5	4	3	2	1	Bit 0
	Reserved			R	NGSE	R	GPDCE	G1LM
Reset	0	0	0	0	0	0	1	0

Bits 7–5 **Reserved (always reads 0)**

Bit 4 **Reserved (RW0)**—This bit must remain 0 for proper operation.

Bit 3 **Non-GART Snoop Enable (RW)**

0 = When clear, AGP addresses that fall outside of the GART range do not cause probes (default)
1 = When set, this bit forces AGP accesses that are not in the GART range to initiate AMD Athlon system bus probes to the processor(s)

Bit 2 **Reserved (RW0)**—This bit is always set to 0 for proper operation.

Bit 1 **GART Page Directory Cache Enable**

0 = GART page directory cache disabled.
1 = GART page directory cache enabled (default).

Bit 0 **Config 1 Level Indexing**

0 = Two-level GART indexing mode (default).
1 = One-level GART indexing mode.

7.4 Device 1 Registers (AGP and PCI-to-PCI Bridge)

These registers configure AGP and secondary PCI bus operation.

Vendor ID — Device 1 — Offset 01h–00h

	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
	Vendor ID															
Reset	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0

This read-only value is defined as 1022h to indicate AMD.

Device ID — Device 1 — Offset 03h–02h

	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
	Device ID															
Reset	0	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1

This read-only value of 7007h represents the AMD-751 system controller PCI-to-PCI bridge in the single processor device.

AGP/PCI Command — Device 1 — Offset 05–04h

	Bits 15–10						9	8	7	6	5	4	3	2	1	Bit 0
	Reserved						FBBE	SERRE	AS	PEEn	VPS	MWI	SC	AIA	AMSE	IOSE
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15–10 Reserved (always reads 0)

Bit 9 **Fast Back-to-Back Enable (always reads 0)**—This bit indicates that fast back-to-back transactions are only allowed to the same agent.

Bit 8 **SERR# Enable (RW)**—This bit and bit 6 must be set to 1 to report address parity errors. ASERR# is an input to the AMD-751 system controller. The AMD-751 receives ASERR# in the AGP timing domain and passes it onto the PCI SERR# so that the AMD-756 peripheral bus controller may generate an interrupt.

0 = SERR# driver disabled (default)
1 = SERR# driver enabled

Note: *If a system error occurs, SERR# may be asserted by an AGP master.*

Bit 7 **Address Stepping (always reads 0)**—This device does not support address stepping.

Bit 6 **Parity Error Enable (always reads 0)**

0 = Parity error checking is not supported

Bit 5 **VGA Palette Snoop (always reads 0)**—Palette accesses generate normal PCI cycles. Palette snooping of AGP devices is not supported.

Bit 4 **Memory Write-and-Invalidate (MWI) Command (always reads 0)**—PCI-to-PCI bridges like the AMD-751 system controller implement this bit as read only.

0 = The AMD-751 does not generate MWI commands

Bit 3 **Special Cycle (always reads 0)**—A PCI-to-PCI bridge never responds as a target to special cycle transactions.

Bit 2 **AGP Initiator Access (RW)**—This bit enables the AGP initiator (graphics controller) to access memory and the system PCI bus.

0 = Disable master accesses from the APCI bus (default)
1 = Enables the AMD-751 to accept master accesses from the APCI bus

Bit 1 **AGP Memory Space Enable (RW)**—By default, the processor writes to graphics adapter memory on PCI bus 0. Setting this bit allows the processor (and PCI masters) to write to graphics adapter memory on the AGP bus. APCI memory space is defined by Device 1, Offset 20 on page 168.

0 = Primary PCI bus (default)
1 = AGP bus/secondary PCI bus

Bit 0 **I/O AGP Enable (RW)**—By default, the processor writes to graphics adapter I/O space on PCI bus 0. Setting this bit allows the processor to write to graphics adapter I/O space on the AGP bus.

0 = Primary PCI bus (default)
1 = AGP bus/secondary PCI bus

When set, the AMD-751 system controller forwards AMD Athlon system bus accesses that reference APCI I/O space onto the APCI. APCI I/O space is defined by Device 1, Offset 1C on page 166.

Status — Device 1 Offset 07h–06h

	Bit 15	14	13	12	11	10–9	8	7	6	5	Bits 4–0
	DPE	ASERR#	RIA	RTA	STA	DEVSEL# Timing	PPE	FBBC	UDF	66 MHz	Reserved
Reset	0	0	0	0	0	0 1	0	0	0	1	0 0 0 0 0

Bit 15 **DRAM Parity Error Detected (always reads 0)**—The AMD-751 system controller does not support parity checking.

Bit 14 **ASERR# Error Detected (RWC)**

0 = No error detected
1 = ASERR# error detected. A device has asserted the ASERR# pin. The AMD-751 then asserts SERR#.

Bit 13 **Received Initiator Abort (RO)**—This bit is set by a PCI initiator when its transaction is terminated with initiator abort.

0 = PCI transactions proceeding normally
1 = The AMD-751 has detected that a transaction was terminated before completion

Bit 12 **Received Target Abort (RO)**—The target issues a target abort when it detects a fatal error or cannot complete a transaction. This bit is set by simultaneously deasserting DEVSEL# and asserting STOP#.

0 = No abort received
1 = Transaction aborted by target

Bit 11 **Signaled Target Abort (always reads 0)**—This AMD-751 system controller never signals a target abort.

Bits 10–9 **DEVSEL# Timing (RO)**—This field indicates the DEVSEL# timing.

00 = Fast
01 = Medium (The AMD-751 only implements this timing)
10 = Slow
11 = Reserved

Bit 8 **PCI Parity Error Detected (always reads 0)**—The AMD-751 system controller does not support parity checking.

Bit 7 **Fast Back-to-Back Capability (always reads 0)**—The AMD-751 can accept fast back-to-back transactions only if they are from the same agent.

Bit 6 **User-Defined Features (always reads 0)**—The AMD-751 system controller does not support user-defined features.

Bit 5 **66 MHz-Capable PCI Bus (always reads 1)**—The APCI (AGP) interface supports 66-MHz operation.

Bits 4–0 **Reserved (always reads 0)**

AGP Revision ID — Device 1 Offset 08h

	Bit 7	6	5	4	3	2	1	Bit 0
	Revision ID							
Reset	0	0	0	0	0	0	0	0

Bits 7–0 **AMD-751 System Controller Revision Code (RO)**—00h = Revision A

Programming Interface — Device 1 Offset 09h

	Bit 7	6	5	4	3	2	1	Bit 0
	Programming Interface							
Reset	0	0	0	0	0	0	0	0

Bits 7–0 **Programming Interface (always reads 0)**—00h = Bridge

Subclass Code — Device 1 Offset 0Ah

	Bit 7	6	5	4	3	2	1	Bit 0
	Subclass Code							
Reset	0	0	0	0	0	1	0	0

Bits 7–0 **Subclass Code (always reads 04h)**—The PCI-defined subclass code for a PCI-to-PCI bridge is 04h.

Base Class Code — Device 1 Offset 0Bh

	Bit 7	6	5	4	3	2	1	Bit 0
	Base Class Code							
Reset	0	0	0	0	0	1	1	0

Bits 7–0 **Base Class Code (always reads 06h)**—The PCI-defined base class code for a bridge device is 06h.

AGP Header Type — Device 1 Offset 0Eh

	Bit 7	6	5	4	3	2	1	Bit 0
	Header Type							
Reset	1	0	0	0	0	0	0	1

Bits 7–0 Header Type (always reads 81h)

AGP Primary Bus Number — Device 1 Offset 18h

	Bit 7	6	5	4	3	2	1	Bit 0
	Primary Bus Number							
Reset	0	0	0	0	0	0	0	0

Bits 7–0 Primary Bus Number (RW)—This field records the number of the PCI bus to which the primary interface of the bridge is connected. The bridge uses this number to decode type 1 configuration transactions on the secondary interface that should be converted to special cycle transactions on the interface.

AGP Secondary Bus Number — Device 1 Offset 19h

	Bit 7	6	5	4	3	2	1	Bit 0
	Secondary Bus Number							
Reset	0	0	0	0	0	0	0	0

Bits 7–0 Secondary Bus Number (RW)—This field records the number of the PCI bus to which the secondary interface of the bridge is connected. The bridge uses this number to determine when to respond to type 1 configuration transactions on the primary interface and convert them to type 0 transactions on the secondary interface.

AGP Subordinate Bus Number — Device 1 Offset 1Ah

	Bit 7	6	5	4	3	2	1	Bit 0
	Subordinate Bus Number							
Reset	0	0	0	0	0	0	0	0

Bits 7–0 Subordinate Bus Number (RW)—This binary number is the system-assigned number of the highest ranking PCI bus subordinate to a PCI bridge.

This field records the number of the highest numbered PCI bus that is behind (or subordinate to) a bridge. The bridge uses this field in conjunction with the secondary bus number register to determine when to respond to type 1 configuration transactions on the primary interface and to pass them on to the secondary interface.

AGP Secondary Latency Timer — Device 1 Offset 1Bh

	Bit 7	6	5	4	3	2	1	Bit 0
	Secondary Latency Timer							
Reset	0	0	0	0	0	0	0	0

Bits 7–0 **Secondary Latency Timer (RW)**—This 8-bit binary value specifies the latency timer for the secondary PCI bus in units of PCI bus clocks.

00000000 = 0 PCI clocks
00000001–11111111 = (8 bit binary value) x PCI clocks

I/O Base Register — Device 1 Offset 1Ch

	Bit 7	6	5	4	3	2	1	Bit 0
	I/O Base Address Lower Nibble				I/O Base RO			
Reset	1	1	1	1	1	1	1	1

Bits 7–4 **I/O Base Address Lower Nibble (RW)**—These four bits determine A[15:12] of the lower boundary of the address range in which the AMD-751 system controller forwards I/O transactions from one interface to the other. A[31:16] are specified in Device 1, Offset 31h–30h (see page 169). The default of Fh disables the forwarding of I/O transactions.

Bits 3–0 **I/O Base Decode Width (RO)**—These bits are set to indicate that 32-bit address decoding is available for I/O.

I/O Limit Register — Device 1 Offset 1Dh

	Bit 7	6	5	4	3	2	1	Bit 0
	I/O Limit Address Lower Nibble				I/O Limit RO			
Reset	0	0	0	0	1	1	1	1

Bits 7–4 **I/O Limit Address Lower Nibble (RW)**—These four bits determine A[15:12] of the upper boundary of the address range in which the AMD-751 system controller forwards I/O transactions from one interface to the other. A[31:16] are specified in Device 1, Offset 33h–32h (see page 169).

Bits 3–0 **I/O Limit Decode Width (RO)**—These bits are set to indicate that 32-bit address decoding is available for I/O.

AGP/PCI Secondary Status — Device 1 Offset 1Fh–1Eh

	Bit 15	14	13	12	11	Bits 10–9	8	7	6	5	Bits 4–0
	DPE	SSE	RIA	RTA	STA	DEVSEL# Tmg	DPED	FBBC	UDF	66 MHz	Reserved
Reset	0	0	0	0	0	0 1	0	0	0	1	0 0 0 0 0

Bit 15 **Detected Parity Error (always reads 0)**—The AMD-751 does not support parity checking.

Bit 14 **Signaled System Error (RWC)**—The AMD-751 system controller sets this bit when ASERR# is sampled asserted by an AGP device. It then asserts SERR#.

0 = No error detected (default)
1 = System error on AGP

Bit 13 **Received Initiator Abort (RWC)**—This bit is set by an AGP initiator whenever its transaction is terminated with initiator abort.

0 = AGP transactions proceeding normally
1 = The AMD-751, acting as a PCI initiator on the AGP bus, has terminated a transaction before completion

Bit 12 **Received Target Abort (RWC)**—The target issues a target abort when it detects a fatal error or cannot complete a transaction by simultaneously deasserting DEVSEL# and asserting STOP#. The AMD-751 sets this bit when it detects this condition on the secondary PCI bus.

0 = No abort received
1 = Transaction aborted by target

Bit 11 **Signaled Target Abort (always reads 0)**—The AMD-751 system controller does not terminate transactions with target aborts.

Bits 10–9 **DEVSEL# Timing (RO)**—This field defines the DEVESL# timing.

00=Fast
01=Medium (default). The AMD-751 only supports this timing.
10=Slow
11=Reserved

Bit 8 **Data Parity Error (always reads 0)**—The AMD-751 system controller does not support parity checking.

Bit 7 **Fast Back-to-Back Capablility (always reads 0)**—The AMD-751 can accept fast, back-to-back transactions from the same agent only.

Bit 6 **User-Defined Features (always reads 0)—**The AMD-751 does not support user-defined features**.**

Bit 5 **66-MHz-Capable PCI Bus (always reads 1)—**The maximum secondary PCI bus operating speed is 66 MHz.

Bits 4–0 **Reserved (always reads 0)**

Memory Base — Device 1 Offset 21h–20h

	Bits 15–4												Bits 3–0			
	Memory Base												Reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15–4 **Memory Base (RW)—**This register defines the base address of the nonprefetchable address range used by the AGP target (graphics controller) where control registers and FIFO-like communication interfaces are mapped. Bits [15:4] correspond to address bits [31:20]. The lower 20 bits of the address are assumed to be 00000h. The memory address range adheres to 1-Mbytes alignment and granularity.

Bits 3–0 **Reserved (always reads 0)**

Memory Limit — Device 1 Offset 23h–22h

	Bits 15–4												Bits 3–0			
	Memory Limit												Reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15–4 **Memory Limit (RW)—**This register defines the top address of the nonprefetchable address range used by the AGP target (graphics controller) where control registers and FIFO-like communication interfaces are mapped. The lower 20 bits of the address are assumed to be 0FFFFFh. The memory address range adheres to 1-Mbytes alignment and granularity.

Bits 3–0 **Reserved (RO) (always reads 0)**

AGP/PCI Prefetchable Memory Base — Device 1 Offset 25h–24h

	Bits 15–4												Bits 3–0			
	Prefetchable Memory Base												Reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15–4 **Memory Base (RW)**—This register defines the base address of the prefetchable address range used by the AGP target (graphics controller) where control registers and FIFO-like communication interfaces are mapped. Bits [15:4] correspond to address bits [31:20]. The lower 20 bits of the address are assumed to be 00000h. The memory address range adheres to 1-Mbyte alignment and granularity.

Bits 3–0 **Reserved (always reads 0)**

AGP/PCI Prefetchable Memory Limit — Device 1 Offset 27h–26h

	Bits 15–4												Bits 3–0			
	Prefetchable Memory Limit												Reserved			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15–4 **Memory Limit (RW)**—This register defines the top address of the prefetchable address range used by the AGP target (graphics controller) where control registers and FIFO-like communication interfaces are mapped. Bits [15:4] correspond to address bits [31:20]. The lower 20 bits of the address are assumed to be 0FFFFFh. The memory address range adheres to 1-Mbyte alignment and granularity.

Bits 3–0 **Reserved (always reads 0)**

I/O Base — Device 1 Offset 30h

	Bit 7	6	5	4	3	2	1	Bit 0
	I/O Base							
Reset	1	0	0	0	0	0	0	1

Bits 7–0 **I/O Base (RW)**—This register defines the top address bits A[23:16] of a 24-bit I/O base address.

Processor addresses that fall between the base and limit specified in this register are passed to the AGP/APCI bus (when the enable bit in Device 1, Offset 04, bit 0 is set).

I/O Limit — Device 1 Offset 32h

	Bit 7	6	5	4	3	2	1	Bit 0
	I/O Limit							
Reset	1	0	0	0	0	0	0	1

Bits 7–0 **I/O Limit (RW)**—This register defines the top address bits A[23:16] of a 24-bit I/O limit address.

Interrupt Control — Device 1 Offset 3Dh–3Ch

	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Interrupt Pin								Interrupt Line							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15–8 **Interrupt Pin (RW) default 00h**—This field indicates which interrupt pin the PCI-to-PCI bridge uses. This field is RW to allow BIOS software to program the required value.

00h = No interrupt channel assigned (default)
01h = INTA#
02h = INTB#
03h = INTC#
04h = INTD#
05h–FFh = Not allowed

Bits 7–0 **Interrupt Line (RW)**—This field is RW to allow BIOS software to program the required value. This register indicates to which input of the system interrupt controller the interrupt signal pin is connected.

00h = Default
01h = INT1
02h = INT2
. . .
0Fh = INT15
10h–FEh = Not allowed
FFh = No interrupt channel assigned (default)

PCI-to-PCI Bridge Control — Device 1 Offset 3Fh–3Eh

	Bit 15	14	13	12	Bits 11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								FB2B	SBR	IAM	R	VGAE	ISAE	SEN	PEE
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: *Although required by the PCI-PCI bridge specification, this register is not used.*

Bits 15–8 Reserved (always reads 0)

Bit 7 **Fast Back-to-Back Enable (always reads 0)**—Fast back-to-back transactions to different devices on the secondary interface are not supported.

Bit 6 **Secondary Bus Reset (always reads 0)**—This bit is not implemented.

Bit 5 **Initiator Abort Mode (always reads 0)**—Determines the behavior of the PCI-to-PCI bridge when a master abort termination occurs on either interface when the bridge is the master of the transaction. Read transactions return all bits equal to 1b, and write data is accepted by the bridge and then dropped. A master abort is not reported.

Bit 4 Reserved (always reads 0)

Bit 3 **VGA Enable (RW)**—When this bit is set, the AMD-751 system controller decodes and forwards VGA accesses to the secondary PCI bus rather than the primary PCI bus. VGA accesses include memory accesses in the range A0000–BFFFFh and I/O addresses in the ranges 3B0h–3BBh and 3C0–3DFh.

0 = VGA accesses are forwarded to the primary PCI bus (default)
1 = VGA accesses are forwarded to the secondary PCI bus

Bit 2 **ISA Enable (RW)**—This bit modifies the response by the bridge to ISA I/O addresses, which applies only to I/O addresses that are enabled by the I/O base and I/O limit registers and are in the first 64 Kbytes of PCI I/O address space (0000_0000h to 0000_FFFFh). When set, the bridge blocks any forwarding from the primary PCI bus to the secondary PCI bus of I/O transactions addressing the last 768 bytes in each 1-Kbyte block. In the opposite direction (secondary to primary), I/O transactions are forwarded if they address the last 768 bytes in each 1-Kbyte block.

0 = Forward all I/O addresses in the address range defined by the I/O base and I/O limit registers (default)
1 = Block forwarding of ISA I/O addresses in the address range defined by the I/O base and I/O limit registers in the first 64 Kbytes of PCI I/O address space (top 768 bytes of each 1-Kbyte block)

Bit 1 **SERR# Enable (RW)**

0 = SERR# assertions on the secondary bus are not forwarded to the primary bus (default)
1 = SERR# assertions on the secondary bus are forwarded to the primary interface

Bit 0 **Parity Error Enable (always reads 0)—**(Secondary bus) The AMD-751 system controller does not support parity checking.

7.5 Memory-Mapped Control Registers

The AMD-751 system controller implements a set of memory-mapped registers to control AGP functionality. The system BIOS determines the base address of these registers and loads that value in the BAR1 configuration register, Device 0, Offset 14h (see page 136).

Features and Capabilities Register — BAR1 + Offset 01h–00h

	Bits 15–12				Bit 11	Bit 10	Bit 9	Bit 8	Bits 7–0							
	Reserved				GHng	PPC	MPC	VC	Revision ID							
Reset	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1

Bits 15–12 Reserved (always reads 0)

Bit 11 Enable Hang on Invalid GART Entries—This bit is used as a test mode to allow the AMD-751 system controller to hang on invalid GART entries. This bit is for software debug purposes only. For normal operation, do not set this bit.

Note: *The enable hang on invalid GART entries test mode is available on the AMD-751 system controller Revision C and later. In previous revisions, this bit is read-only and always reads 0.*

Bit 10 PCI-to-PCI Capability (RO)—This bit is cleared to indicate that the AMD-751 only implements those PCI-to-PCI bridge commands required to implement AGP. (The AMD-751 does not implement a complete PCI 2.2-compliant PCI-to-PCI bridge between the PCI bus and AGP.)

Bit 9 Multiple Pages Capability (always reads 1)—This bit is set to indicate that the AMD-751 system controller supports multiple GART page entries.

Bit 8 Valid Bit Error Capability (always reads 1)—This bit is set to indicate that the AMD-751 supports the detection of valid bit errors. The controller detects an access to an invalid page by checking the valid bit for each page of the GART.

Bits 7–0 Revision ID (always reads 01h)

Enable and Status Register — BAR1 + Offset 03h–02h

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bits 7–4	Bit 3	Bit 2	Bit 1	Bit 0
	Reserved				PPS	GCS	MPS	VBES	Reserved	PPE	GCE	EnSb Detect	VBEE
Reset	0	0	0	0	0	0	0	0	0 0 0 0	0	0	0	0

Bit 15–12 Reserved (always reads 0)

Bit 11 PCI-to-PCI Status (always reads 0)—This bit is cleared to indicate that the AMD-751 system controller only implements those PCI-to-PCI bridge commands required to implement AGP. (The AMD-751 does not implement a complete PCI 2.2-compliant PCI-to-PCI bridge between the PCI bus and AGP.)

Bit 10 GART Cache Status (RO)

0 = GART cache is disabled (default)
1 = GART cache has been enabled by software (see description of bit 2 below)

Bit 9 Multiple Page Status (RO)—This bit is always 0 for the AMD-751 Revision C3 and later.

0 = Variable number of pages per GART directory cache (GDC) entry are disabled. Each GDC entry cached refers to one 4-Kbyte page only. (default)
1 = Variable number of pages per GDC entry are enabled. Each GDC entry cached refers to multiple 4-Kbyte pages. (Not supported)

Bit 8 Valid Bit Error Status (RO)—The AMD-751 system controller sets this bit when the GART attempts to access an invalid page. If valid bit error signalling is enabled (bit 0 is set), the system also asserts SERR#.

0 = No error detected (default)
1 = Valid bit error detected

Bits 7–4 Reserved (always reads 0)

Bit 3 PCI-to-PCI Enable (always reads 0)—This bit is cleared to indicate that the AMD-751 system controller only implements the PCI-to-PCI bridge commands required to implement AGP. (The AMD-751 does not implement a complete PCI 2.2-compliant PCI-to-PCI bridge between the PCI bus and AGP.)

Bit 2 Gart Cache Enable (RW)

0 = GART translation lookaside buffer (TLB) entry caching disabled (default)
1 = GART TLB entry caching enabled

Bit 1 Disable SB_SBA Detect Logic (RW)—Setting this bit disables the automatic SB_SBA strobe detect logic. For backwards compatibility, the power-on default condition for this bit is 0 (Enable Detect Logic). BIOS and any driver that writes to this register should set this bit to a 1 (disable) state only on the AMD-751 Revision C3 and later.

Note: *Enable SB_SBA Detect Logic is available on the AMD-751 system controller Revision C3 and later. This newly defined control bit replaces a previously existing control in this register, "Multiple Pages Enabled", which enabled multiple pages per GART entry. That feature is not supported and bit 9 always read 0.*

Bit 0 Valid Bit Error Enable (RW)—Setting this bit enables assertion of SERR# when a graphics device attempts to access a page in AGP memory that is not valid (page fault), generating a valid bit error.

0 = SERR# is not asserted on a valid bit error (default)
1 = SERR# is asserted on a valid bit error

AGP GART Base Address Register — BAR1 + Offset 07h–04h

Bits 31–12	Bits 11–0
GART Base Address	Reserved

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 31–12 Base Address High (RW) (Default 00000h)—These 20 bits correspond to the 20 most-significant bits of the 32-bit GART base address, which is aligned on a 4-Kbyte page boundary. These 20 bits provide 4-Kbyte resolution, the minimum allowable size of the GART. A value other than 0 defines a valid base address.

Bits 11–0 Reserved (always reads 0)

GART Cache Size Register — BAR1 + Offset 0Bh–08h

Bits 31–0
GART Cache Size

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits 31–0 Cache Size (always reads 02h)—The AMD-751 system controller implements a GART cache that contains 16 entries, organized as 8-way, two set-associative.

GART Cache Control Register — BAR1 + Offset 0Fh–0Ch

	Bits 31–1	0
	Reserved	Inv
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0

Bits 31–1 Reserved (always reads 0)

Bit 0 GART Cache Invalidate (RW) default 0—The AGP driver sets this bit to invalidate the entire GART cache. When the AMD-751 system controller samples the bit High, it invalidates the cache and clears the bit.

GART Entry Control Register — BAR1 + Offset 13h–10h

	Bits 31–12	Bits 11–2	Bit 1	Bit 0
	GART Entry Offset	Reserved	Updt	Inv
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0	0	0

Bits 31–12 GART Entry Offset (RW) (default 00000h)—To invalidate or update an entry in the GART cache, bits 31–12 are written with the most significant 20 bits of the virtual address. If this address is present in the GART cache, it is invalidated or updated based on the state of bits 1–0. If the address written to bits 31–12 is either outside of the GART aperture or not present in the GART cache, no action is taken.

Bits 11–2 Reserved (always reads 00h)

Bit 1 GART Cache Entry Update (RW) (default 0)—Setting this bit forces the AMD-751 system controller to update the GART cache entry specified in bits A[31:12] with the current entry in the GART table in system memory. The update function is performed immediately following the write to this register. The bit is cleared when the update operation is completed.

Bit 0 GART Cache Entry Invalidate (RW) (default 0)—Setting this bit forces the AMD-751 to invalidate the GART cache entry specified in bits [31:12] if they are present in the GART cache. The invalidate function is performed immediately following the write to this register. The bit is cleared when the invalidate operation is completed.

Note: *Bits 1–0 must never be set (11b) simultaneously.*

00 = No action (default)
01 = Invalidate
10 = Update
11 = Not allowed

PM2 (Power Management) — BAR2 + Offset 04h–00h

	Bits 31–1	Bit 0
	Reserved	ArbD
Reset	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	

Bits 31–1 Reserved (always reads 0)

Bit 0 Arbiter Disable (RW)—This bit is used to enable and disable the system arbiter.

0 = The system arbiter is enabled and the arbiter can grant bus ownership to other bus masters in the system (default)

1 = When this bit is High, the system arbiter is disabled and the boot processor (given in WHAMI—Device 0, Offset 80—see page 151) has ownership of the system. AGP and PCI masters are not granted ownership of the bus.

8 Electrical Data

8.1 Absolute Ratings

The AMD-751 system controller is not designed to operate beyond the parameters shown in Table 24.

WARNING: ***The absolute ratings in Table 24 and associated conditions must be adhered to in order to avoid damage to the AMD-751 system controller and motherboard. Systems using the AMD-751 must be designed to ensure that the power supply and system logic board guarantee that these parameters are not violated. VIOLATION OF THE ABSOLUTE RATINGS WILL VOID THE PRODUCT WARRANTY.***

Table 24. Absolute Ratings

Parameter	Minimum	Maximum	Comments
V_{DD}	–0.5 V	3.6 V	Core and I/O Supply
REF_5V	–0.5 V	5.5 V	Reference Supply
V_{DD} > REF_5V		1.0 V	1mS max. excursion
V_{PIN} SDRAM	–0.5 V	V_{DD} + 0.5 V	
V_{PIN} Processor	–0.5 V	3.0 V	
V_{PIN} PCI	–0.5 V	REF_5V + 0.5 V	
V_{PIN} AGP	–0.5 V	V_{DD} + 0.5 V	
T_{CASE} (under bias)	0 °C	70 °C	
$T_{STORAGE}$	–55 °C	+125 °C	

8.2 Operating Ranges

The AMD-751 system controller is designed to provide functional operation if the voltage and temperature parameters are within the limits defined in Table 25.

Table 25. Operating Ranges

Parameter	Minimum	Typical	Maximum	Comments
REF_5V	4.5 V	5.0 V	5.5 V	5 Volt Reference
V_{DD}	3.14 V	3.3V	3.46 V	Core (+/– 5%)
T_{CASE}	0 °C		85°C	

Note: *The voltage applied to V_{DD} should never exceed the voltage applied to REF_5V.*

8.3 DC Characteristics

Table 26 shows the DC characteristics for the AMD-751 system controller. Table 27 on page 182 shows the DC characteristics for the AMD Athlon system bus/AMD-751.

Table 26. DC Characteristics

Symbol	Parameter Description	Preliminary Data		Comments
		Min	Max	
V_{IL}	Input Low Voltage (LVTTL Inputs)	–0.5 V	0.8 V	
V_{IH}	Input High Voltage (LVTTL Inputs)	2.0 V	5.5 V	
V_{OL}	Output Low Voltage (LVTTL Outputs)		0.45 V	
V_{OH}	Output High Voltage (LVTTL Outputs)	2.4 V		
I_{REF_5V}	5-V Power Supply Current		1 mA	
I_{DD}	3-V Power Supply Current (Dynamic)	1.1 A	1.5 A	
I_{LI}	Input Leakage Current		10 µA	
I_{LO}	Output Leakage Current		10 µA	
I_{IL}	Input Leakage Current Bias with Pullup		40 µA	
I_{IH}	Input Leakage Current Bias with Pulldown		–40 µA	
C_{IN}	Input Capacitance		10 pF	
C_{OUT}	Output Capacitance		15pF	
C_{OUT}	I/O Capacitance		20pF	

Table 27. AMD Athlon™ System Bus/AMD-751™ System Controller DC Specification

Symbol	Parameter Description	Minimum	Nominal	Maximum	Units	Notes
VccCore	DC Supply Voltage	1.3	1.5	1.7	V	
V_{REF}	DC Input Reference Voltage	(0.6*VccCore) –50	0.6*VccCore	(0.6*VccCore) +50	mV	1
I_{VREF}	DC Reference Current	–50	–	50	µA	2
V_{IH} (DC)	DC Input High Voltage	VREF + 100	–	VccCore + 300	mV	
V_{IL} (DC)	DC Input Low Voltage	–300	–	VREF – 100	mV	
V_{IH} (AC)	AC Input High Voltage	VREF + 200	–	VccCore + 500	mV	
V_{IL} (AC)	AC Input Low Voltage	–500	–	VREF – 200	mV	
V_{OH} (DC)	DC Output High Voltage	VccCore	–	VccCore + 300	mV	
V_{OL} (DC)	DC Output Low Voltage	–300	–	400	mV	
V_{OH} (AC)	AC Output High Voltage	VccCore	–	VccCore + 500	mV	
V_{OL} (AC)	AC Output Low Voltage	–500	–	400	mV	
I_{LEAK}	Tristate Leakage	–10	–	10	µA	
I_{IH}	Input High Current	–10	–	10	µA	3
I_{IL}	Input Low Current	–10	–	10	µA	3
I_{OL}	Output Low Current	33	–	–	mA	3

Notes:

** See Figure 34 on page 194 for more information about the test circuit.*

1. *V_{REF}:*
   - *V_{REF} is nominally set by a (1%) resistor divider from VccCore.*
   - *The suggested divider resistor values are 80.6 ohms over 121.0 ohms to produce a divisor of 060.*
   - *Given: VccCore = 1.6 V, V_{REF} = 960mV (1.6 * 0.60).*
   - *Peak to Peak AC noise on V_{REF} (AC) should not exceed 2% of V_{REF} (DC).*
2. *I_{VREF} should be measured at nominal V_{REF}.*
3. *I_{IH}, I_{IL}, and I_{OL} are measured at V_{IH}-MIN (DC), V_{IL}-MAX (DC), and V_{OL}-MAX (DC) respectively.*

8.4 Power Dissipation

Table 28 shows typical and maximum power dissipation of the AMD-751 system controller during normal and reduced power states. The measurements are taken with the V_{DD} shown.

Table 28. Typical and Maximum Power Dissipation

Clock Control State	Typical @ 100 MHz	Maximum @ 100 MHz	Comments
Normal (Thermal Power)	4.3 W @ 3.3 V	5.25 W @ 3.5 V	
Halt-Disconnect	3.3 W @ 3.3 V	3.85 V @ 3.5 V	With SYSCLK running

8.4.1 Thermal Considerations

To allow for proper cooling and to maintain the case temperature specified in Table 24 on 179, the AMD-751 system controller requires a heatsink. Table 29 and Table 30 list recommended heatsinks and thermal materials, respectively.

Table 29. Heatsinks for the AMD-751™ System Controller

Vendor	Part Number
Aavid	372924M02000
Foxconn	PHC0802-071

Table 30. Thermal Interface Material for the AMD-751™ System Controller

Vendor	Part Number
Chomerics	T710 *
Furon	FC1060
Furon	C960*
Furon	C964
Furon	C965
Bergquist	200G
Thermagon	T-pcm708
Thermagon	T-pcm910

Notes:
* *An adhesive is included for easy attachment*

9 Switching Characteristics

The AMD-751 system controller signal switching characteristics are presented in Tables 31 through 37. Valid delay, float, setup, and hold timing specifications are listed.

All signal timings are based on the following conditions:

- The target signals are input or output signals that are switching from logical 0 to 1, or from logical 1 to 0.
- Measurements are taken from the time the reference signal (ACLK, PCLK, SDRAM CLK_IN, SYSCLK or RESET) passes through 1.5V to the time the target signal passes through 1.5V.
- Parameters are within the range of those listed in "Operating Ranges" on page 180.

9.1 SYSCLK Switching Characteristics

Table 31 contains the switching characteristics of the SYSCLK input to the AMD-751 system controller for 100-MHz processor bus operation. These timings are all measured with respect to the voltage levels indicated by Figure 31. Table 32 on page 187 contains the switching characteristics of the A_CLK input for 66-MHz PCI bus operation. Table 33 on page 187 contains the switching characteristics of the PCLK input for 33-MHz PCI bus operation. These timings are all measured with respect to the voltage levels indicated by Figure 32 on page 187.

The CLK period stability specifies the variance (jitter) allowed between successive periods of the CLK input measured at appropriate reference voltage. This parameter must be considered as one of the elements of clock skew between the AMD-751 and the system logic.

Table 31. SYSCLK Switching Characteristics for 100-MHz Bus Operation

Symbol	Parameter Description	Preliminary Data		Figure	Comments
		Min	Max		
$1/t_2$	Frequency		100 MHz	31	
t_3/t_2 x 100	SYSCLK Duty Cycle	45%	55%	31	1.15V Reference
t_4	SYSCLK Falling Edge Slew Rate		1.0 V/ns	31	
t_5	SYSCLK Rising Edge Slew Rate		1.0 V/ns	31	
	SYSCLK Period Stability		± 250 ps		1.15V Reference

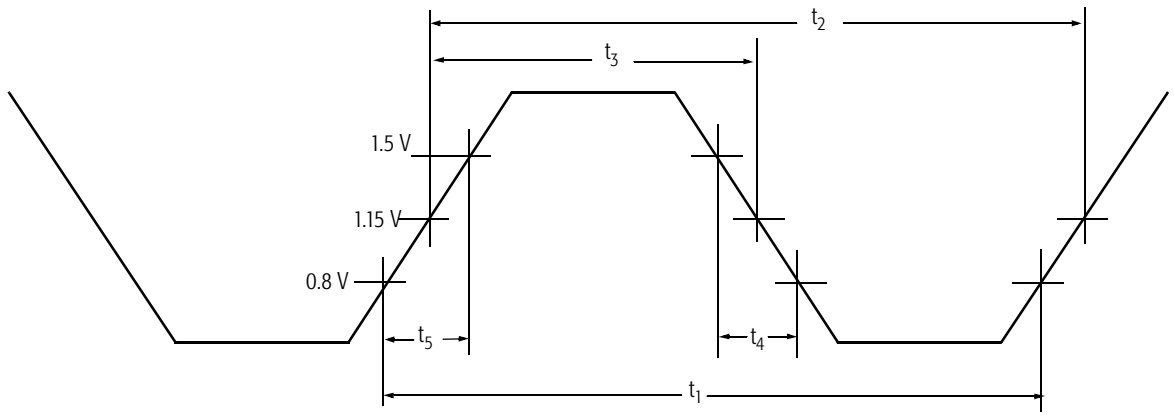


Figure 31. SYSCLK Waveform

Table 32. A_CLK Switching Characteristics for 66-MHz Bus Operation

Symbol	Parameter Description	Preliminary Data		Figure	Comments
		Min	Max		
	Frequency		66 MHz		
t_2	A_CLK High Time	6.0 ns		32	
t_3	A_CLK Low Time	6.0 ns		32	
t_4	A_CLK Fall Time	0.15 ns	1.5 ns	32	
t_5	A_CLK Rise Time	0.15 ns	1.5 ns	32	
	A_CLK Period Stability		± 250 ps		1.5V Reference

Table 33. PCLK Switching Characteristics for 33-MHz PCI Bus

Symbol	Parameter Description	Preliminary Data		Figure	Comments
		Min	Max		
t_1	PCLK Cycle	30 ns	∞	32	
t_2	PCLK High Time	11.0 ns		32	
t_3	PCLK Low Time	11.0 ns		32	
t_4	PCLK Fall Time	1 V/ns	4V/ns	32	
t_5	PCLK Rise Time	1 V/ns	4V/ns	32	
	PCLK Period Stability		± 250 ps		1.5V Reference

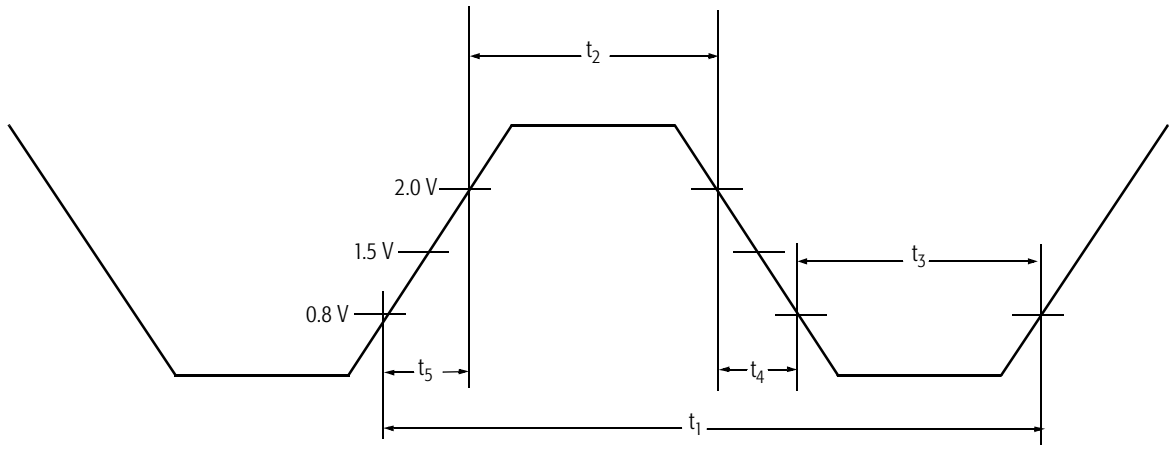


Figure 32. CLK Waveform

9.2 Valid Delay, Float, Setup, and Hold Timings

The valid delay and float timings for output signals during functional operation are relative to the rising edge of the given clock. The maximum valid delay timings are provided to allow a system designer to determine if setup times can be met. Likewise, the minimum valid delay timings are used to analyze hold times.

The setup and hold time requirements for the AMD-751 system controller input signals presented here must be met by any device that interfaces with it to assure the proper operation of the AMD-751.

Figure 33 shows the relationship between the rising clock edge and setup, hold, and valid data timings.

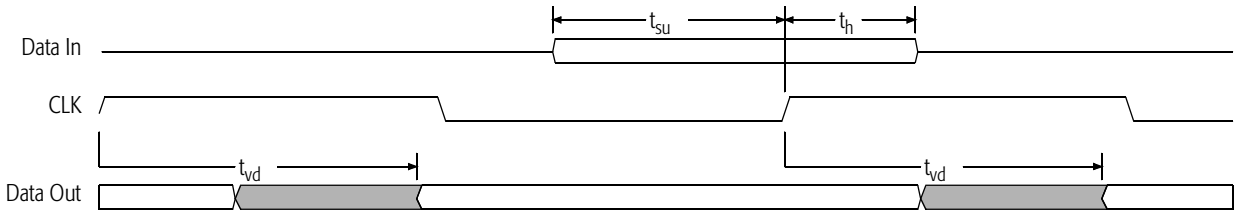


Figure 33. Setup, Hold, and Valid Delay Timings

9.3 PCI Interface Timings

Table 34 shows the PCI interface timings. All of the timings are relative to PCLK.

Table 34. PCI Interface Timings

Symbol	Parameter Description	Preliminary Data		Figure	Comments
		Min	Max		
t_{su}	AD[31:0] Setup Time	7 ns		33	
	PREQ#, REQ[3:0]# Setup Time	12 ns		33	
	Setup Time for FRAME# STOP# TRDY# DEVSEL# IRDY# C/BE[3:0]# RESET#	7 ns		33	
t_h	AD[31:0] Hold Time	0 ns		33	
	Hold Time for FRAME# STOP# TRDY# DEVSEL# IRDY# C/BE[3:0]# PREQ# REQ[3:0]#	0 ns		33	
t_{vd}	AD[31:0] Valid Delay (address phase)	2 ns	11 ns	33	Pad 12 (Note)
	AD[31:0] Valid Delay (data phase)	2 ns	11 ns	33	Pad 12 (Note)
	Valid Delay for FRAME# STOP# TRDY# DEVSEL# IRDY# C/BE[3:0]# GNT[3:0]#	2 ns	11 ns	33	Pad 13 (Note)
	PGNT# Valid Delay	2 ns	12 ns	33	
t_{fd}	Float Delay for FRAME# STOP# TRDY# DEVSEL# IRDY# C/BE[3:0]#		28 ns	33	Note
t_{pw}	RESET# Pulse Width	2 clks		33	
t_{lat}	REQ# to GNT# Latency	3 clks		33	

Note:
Measurements are taken with no load for t_{min}, and 50 pF for t_{max}.

9.4 SDRAM Interface Timings

Table 35 shows the SDRAM interface timings. All of the following timings are relative to SYSCLK, except where noted.

Table 35. DRAM Interface Timing

Symbol	Parameter Description	Preliminary Data		Figure	Comments
		Min	Max		
t_{su}	MDAT[63:0] Setup	2 ns		33	Relative to SDRAM Clk_In (Note 3)
	MECCD[7:0] Setup	2 ns		33	
t_h	MDAT[63:0] Hold	1 ns		33	Relative to SDRAM Clk_In (Note 3)
	MECCD[7:0] Hold	1 ns		33	
t_{vd}	SDRAM Clk_Out Valid Delay	2 ns	6 ns	33	Pad (Note 1 and Note 2)
	CS[5:0]# Valid Delay	2 ns	6 ns	33	Pad (Note 1 and Note 2)
	MCKE[2:0] Valid Delay	2 ns	6 ns	33	Pad (Note 1 and Note 2)
	DQM[7:0]# Valid Delay	2 ns	6 ns	33	Pad (Note 1 and Note 2)
	SRAS[2:0]# Valid Delay	2 ns	6 ns	33	Pad (Note 1 and Note 2)
	SCAS[2:0]# Valid Delay	2 ns	6 ns	33	Pad (Note 1 and Note 2)
	WE[2:0]# Valid Delay	2 ns	6 ns	33	Pad (Note 1 and Note 2)
	MAdA/MAdB[14:0] Valid Delay	2 ns	6 ns	33	Pad (Note 1 and Note 2)
	MD[63:0] Valid Delay	2 ns	6 ns	33	Pad (Note 1 and Note 2)
	MECCD[7:0] Valid Delay	2 ns	6 ns	33	Pad (Note 1 and Note 2)
t_{SKEW}	Controls Outputs	–0.5 ns	1.5 ns		Relative to SDRAM Clk_Out (Note 3)
	MD[63:0] and MECCD[7:0] Outputs	TBD ns	2.0 ns		Relative to SDRAM Clk_Out (Note 3)

Notes:

1. *Measurements are taken with 50 ohm, ~ 30 pF load.*
2. *Measurements for Min. were taken with the drive strength set to light, and measurements for Max. were taken with the drive strength set to high.*
3. *By design, not tested.*

9.5 AGP Interface Timings

The AGP interface can operate in two modes—1x and 2x. The timings for the 1x mode, shown in Table 36, are relative to A_CLK. The timings for the 2x mode, shown in Table 37 on page 192, are relative to the respective strobe.

Table 36. AGP 1x Mode Timings

Symbol	Parameter Description	Preliminary Data		Figure	Comments
		Min	Max		
t_{su}	A_AD[31:0] Setup Time	5.5 ns			Note
	Setup time for A_FRAME# A_STOP# A_TRDY# A_DEVSEL# A_IRDY# A_C/BE[3:0]# A_REQ# ADSTB[1:0] SBA[7:0] SBSTB RBF#	6 ns			Note
t_h	A_AD[31:0] Hold Time	0 ns			Note
	Hold time for A_FRAME# A_STOP# A_TRDY# A_DEVSEL# A_IRDY# A_C/BE[3:0]# A_REQ# ADSTB[1:0] SBA[7:0] SBSTB RBF#	0 ns			Note
t_{vd}	A_AD[31:0] Valid Delay	1 ns	6.0 ns		Note
	A_C/BE[3:0]# Valid Delay	1 ns	5.5 ns		Note
	Valid Delay for A_FRAME# A_STOP# A_TRDY# A_DEVSEL# A_IRDY# A_GNT#	1 ns	5.5 ns		Note
t_{fd}	Float Delay (Active to Float)	1 ns	14 ns		Note
t_{on}	Turn-on Delay (Float to Active)	1 ns	6 ns		Note

Note:
These signals are specified with a 10 pF load.

Table 37. AGP 2x Mode Timings

Symbol	Parameter Description	Preliminary Data		Figure	Comments
		Min	Max		
t_{su}	A_AD[31:0] Setup Time Relative to Strobe	1 ns			Note
	Setup Time Relative to Strobe for A_FRAME# A_STOP# A_TRDY# A_DEVSEL# A_IRDY# A_C/BE[3:0]# A_REQ# SBA[7:0] RBF#	1 ns			Note
t_h	A_AD[31:0] Hold Time Relative to Strobe	1 ns			Note
	Hold time relative to strobe for A_FRAME# A_STOP# A_TRDY# A_DEVSEL# A_IRDY# A_C/BE[3:0]# A_REQ# SBA[7:0] RBF#	1 ns			Note
t_{Datava}	A_AD[31:0] Valid Delay after Strobe	1.9 ns			Note
t_{CBEva}	A_C/BE[3:0]# Valid Delay after Strobe	1.9 ns			Note
t_{Datavb}	A_AD[31:0] Valid before Strobe	1.7 ns			Note
t_{CBEvb}	A_C/BE[3:0]# Valid before Strobe	1.7 ns			Note
t_{fd}	Float Delay (Active to Float)	1 ns	12 ns		Note
t_{on}	Turn-on Delay (Float to Active)	1 ns	9 ns		Note

Note:
These signals are specified with a 10 pF load.

9.6 AMD Athlon™ System Bus Timings

Table 38 shows the AMD Athlon system bus timings. Figure 34 on page 194 shows the test circuit used to achieve the values in the table.

Table 38. AMD Athlon™ System Bus/AMD-751™ System Controller AC Specification

Group	Symbol	Parameter Description	Minimum	Nominal	Maximum	Units	Notes
Clock Forward Group Signals	$T_{NB-SKEW-SAMEEDGE}$	Output skew with respect to the same clock edge	–	–	400	ps	1
	$T_{NB-SKEW-DIFFEDGE}$	Output skew with respect to a different clock edge	–	–	1025	ps	1
	T_{NB-SU}	Input Data Setup Time	500	–	–	ps	1,2
	T_{NB-HD}	Input Data Hold Time	800	–	–	ps	1,2
	T_{RISE}	Signal or Clock Rise Time	1	–	3	V/ns	
	T_{FALL}	Signal or Clock Fall Time	1	–	3	V/ns	
	C_{DATA}	Data Pin Capacitance	4	–	12	pF	
	C_{INCLK}	Input Clock Capacitance	4	–	12	pF	
Sync Signals *3	$T_{NB-SYSCLK-TO-PAD}$	SYSCLK to synchronous signal output at pad (CONNECT, CLKFWDRST)	2400	–	4800	ps	4,5
	$T_{NB-SETUP-TO-SYSCLK}$	Input setup time for synchronous signal to SYSCLK (PROCRDY)	1500	–	–	ps	4,5
	$T_{NB-HOLD-FROM-SYSCLK}$	Input hold time for synchronous signal to SYSCLK (PROCRDY)	1200	–	–	ps	4,5

Notes:

** See Figure 34 on page 194 for more information about the test circuit.*

1. *$T_{NB-SKEW-SAMEEDGE}$ is the maximum skew within a clock forwarded group between any two signals or between any signal and its forward clock, as measured at the package, with respect to the same clock edge.*
   $T_{NB-SKEW-DIFFEDGE}$ is the maximum skew within a clock forwarded group between any two signals or between any signal and its forward clock, as measured at the package, with respect to different clock edges.
2. *Input SU and HLD times are with respect to the appropriate Clock Forward Group input clock.*
3. *The synchronous signals include PROCREADY, CONNECT, and CLKFWDRST.*
4. *This value is measured with respect to the rising edge of SYSCLKIN.*
5. *Test Load—25pF.*

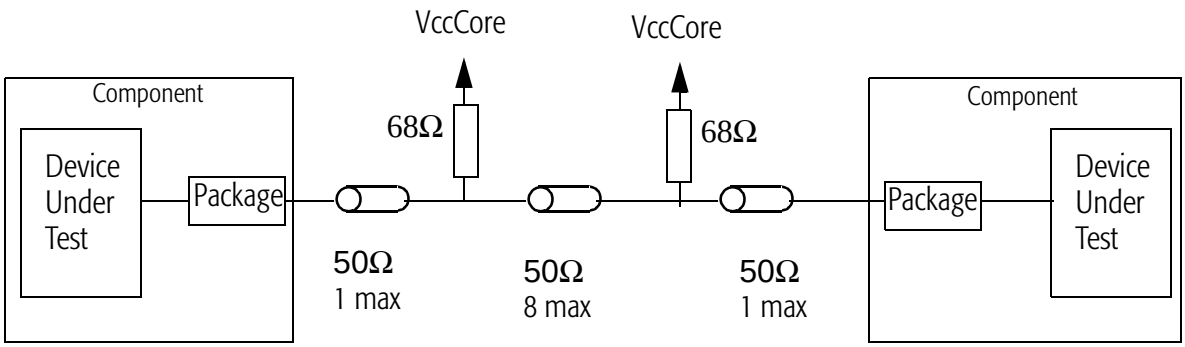


Figure 34. Test Circuit

10 I/O Buffer Characteristics

Except for the AMD Athlon system bus, all of the AMD-751 system controller inputs, outputs, and bidirectional buffers are implemented using a 3.3V buffer design. The AMD Athlon system bus runs at the processor core voltage (nominally 1.6V). AMD has developed a model that represents the characteristics of the actual I/O buffers to allow system designers to perform analog simulations of the AMD-751 system controller signals that interface with the various system components. Analog simulations are used to determine the time of flight of a signal from source to destination and whether the system signal quality requirements are met. Signal quality measurements include overshoot, undershoot, slope reversal, and ringing.

10.1 I/O Buffer Model

AMD provides a model of the AMD-751 system controller I/O buffer for system designers to use in board-level simulations. This I/O buffer model conforms to the *I/O Buffer Information Specification (IBIS)*. The I/O model contains voltage versus current (V/I) and voltage versus time (V/T) data tables for accurate modeling of I/O buffer behavior.

The following list characterizes the properties of the I/O buffer model:

- All data tables contain minimum, typical, and maximum values to allow for worst-case, typical, and best-case simulations, respectively.
- The pullup, pulldown, power clamp, and ground clamp device V/I tables contain enough data points to accurately represent the nonlinear nature of the V/I curves. In addition, the voltage ranges provided in these tables extend beyond the normal operating range of the AMD-751 system controller for those simulators that yield more accurate results based on this wider range.
- The rising and falling ramp rates are specified.

- For most of the drivers, the min/typ/max V_{CC3} operating range is specified as 3.135V, 3.3V, and 3.6V, respectively.
- V_{il} = 0.8V, V_{ih} = 2.0V, and V_{meas} = 1.5V
- For the AMD Athlon system bus, the min/typ/max V_{CC3} operating range is specified as 1.3V, 1.5V, and 1.8V, respectively.
- V_{il} = 1.4V, V_{ih} = 1.8V, and V_{meas} = 1.6V
- The R/L/C of the package is modeled.
- The capacitance of the silicon die is modeled.
- The model assumes a test load resistance of 50Ω for all pins except for the AMD Athlon system bus, which assumes a 34Ω load.

10.2 I/O Model Application Note

For the AMD-751 system controller I/O buffer IBIS model, go to the AMD website at www.amd.com. For background information refer to the *AMD-K6® Processor I/O Model (IBIS) Application Note*, order# 21084.

10.3 I/O Buffer AC and DC Characteristics

See Chapter 9, "Switching Characteristics" starting on page 185 for the AMD-751 system controller AC timing specifications.

See Chapter 8, "Electrical Data" starting on page 179 for the AMD-751 system controller DC specifications.

11 Pin Designations

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	MDAT[47]	MECCD[4]	MECCD[5]	SCAS[0]#	DQM[0]#	DQM[1]#	SRAS[2]#	MAdA[3]	MAdA[5]	MAdA[6]	MAdA[10]	MAdA[11]	CS[5]#	A
B	MDAT[14]	MECCD[0]	MECCD[1]	WE[2]#	DQM[4]#	DQM[5]#	SRAS[0]#	MAdA[0]	MAdA[2]	MAdA[7]	MAdA[8]	MAdA[13]	MAdA[14]	B
C	MDAT[44]	MDAT[13]	VSS	SCAS[2]#	WE[0]#	VSS	CS[1]#	MAdA[1]	VSS	MAdA[4]	MAdA[9]	VSS	CS[4]#	C
D	MDAT[10]	MDAT[42]	MDAT[11]	MDAT[15]	SCAS[1]#	CS[3]#	CS[2]#	SRAS[1]#	MAdB[1]	MAdB[3]	MAdB[5]	MAdB[6]	MAdB[8]	D
E	MDAT[6]	MDAT[39]	MDAT[9]	MDAT[45]	MDAT[46]	WE[1]#	CLKOUT	CLKIN	MAdB[0]	MAdB[2]	MAdB[4]	MAdB[9]	MAdB[7]	E
F	MDAT[5]	MDAT[37]	VSS	MDAT[12]	MDAT[43]	VSS	VSS	VDD	VDD	VDD				F
G	MDAT[34]	MDAT[3]	MDAT[4]	MDAT[40]	MDAT[41]	VSS								G
H	SADDOUT [14]#	MDAT[1]	MDAT[2]	MDAT[38]	MDAT[8]	VDD								H
J	SADDOUT [13]#	VSS	SADDOUT [7]#	MDAT[36]	MDAT[7]	VDD								J
K	SADDOUT CLK#	SADDOUT [12]#	SADDOUT [9]#	MDAT[33]	MDAT[35]	VDD								K
L	SADDOUT [8]#	SADDOUT [5]#	SADDOUT [6]#	MDAT[32]	MDAT[0]						VSS	VSS	VSS	L
M	SADDOUT [2]#	VSS	SADDOUT [10]#	VTERM[6]	SADDOUT [11]#						VSS	VSS	VSS	M
N	SADDOUT [3]#	SDATAOU TCLK[3]#	SCHECK [6]#	SADDOUT [4]#	SDATA [55]#						VSS	VSS	VSS	N
P	SDATA [53]#	SDATA [49]#	SDATA [63]#	SDATA [54]#	SDATA [52]#						VSS	VSS	VSS	P
R	SDATAIN-CLK[3]#	VSS	SDATA [61]#	VTERM[7]	SDATA [50]#						VSS	VSS	VSS	R
T	SDATA [62]#	SDATA [60]#	SCHECK [7]#	SDATA [51]#	SDATA [48]#						VSS	VSS	VSS	T
U	SDATA [59]#	SDATA [58]#	SDATA [57]#	SDATA [36]#	SDATA [46]#	VSS								U
V	SDATA [39]#	VSS	SDATA [37]#	VTERM[8]	SDATA [35]#	VSS								V
W	SDATA [56]#	SDATA [47]#	SDATA [38]#	SCHECK [4]#	SDATA [34]#	VSS								W
Y	SDATA [45]#	SDATA [44]#	SDATAIN-CLK[2]#	SDATA [33]#	SDATA [32]#	VSS								Y
AA	SCHECK [5]#	VSS	SDATAOU TCLK[2]#	VTERM[0]	SDATA [30]#	VSS	VSS	VSS	VSS	VSS				AA
AB	SDATA [43]#	SDATA [42]#	SDATA [41]#	SDATA [31]#	SDATAIN-CLK[1]#	SDATA [28]#	SDATA [27]#	SDATA [24]#	SDATA [1]#	SCHECK [1]#	SDATA [10]#	SADDIN [7]#	SADDIN [8]#	AB
AC	SDATA [40]#	SDATAOU TCLK[1]#	VSS	SCHECK [3]#	SDATA [29]#	VTERM[3]	SDATA [25]#	SDATA [15]#	VTERM[4]	SDATA [8]#	SDATAOU TCLK[0]#	VTERM[1]	SDATAIN-VAL#	AC
AD	VSS	SDATA [23]#	SDATA [19]#	VTERM[5]	SDATA [17]#	SDATA [26]#	SCHECK [0]#	SDATAIN-CLK[0]#	SDATA [12]#	SDATA [14]#	SADDIN [5]#	SADDIN [6]#	SADDIN [4]#	AD
AE	SDATA [22]#	SDATA [21]#	SCHECK [2]#	SDATA [18]#	SDATA [16]#	VSS	SDATA [4]#	SDATA [3]#	VSS	SDATA [11]#	SADDIN [11]#	VSS	SADDIN [10]#	AE
AF	VREF	SDATA [20]#	VSS	SDATA [7]#	SDATA [6]#	SDATA [5]#	SDATA [2]#	SDATA [0]#	SDATA [13]#	SDATA [9]#	SADDIN [2]#	SADDIN [3]#	SADDIN [9]#	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	

	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	MCKE[2]	DQM[2]#	MAdB[12]	MECCD[3]	MDAT[49]	MDAT[19]	MDAT[52]	MDAT[54]	MDAT[24]	MDAT[26]	MDAT[28]	MDAT[29]	MDAT[31]	A
B	MCKE[1]	DQM[3]#	MECCD[2]	MDAT[16]	MDAT[18]	MDAT[51]	MDAT[21]	MDAT[23]	MDAT[25]	MDAT[27]	MDAT[60]	A_CLK	SYSCLK	B
C	CS[0]#	VSS	MECCD[6]	MDAT[17]	VSS	MDAT[20]	MDAT[22]	VSS	MDAT[57]	MDAT[59]	VSS	BYPASS#	S_CLKREF	C
D	MAdB[13]	MAdB[14]	MCKE[0]	DQM[7]#	MECCD[7]	MDAT[50]	MDAT[55]	MDAT[58]	MDAT[62]	REF_5V	S_CLKOUT	PCLK	ROM_SDA	D
E	MAdB[10]	MAdB[11]	DQM[6]#	MAdA[12]	MDAT[48]	MDAT[53]	MDAT[56]	MDAT[61]	MDAT[63]	MDAT[30]	DCSTOP#	RESET#	A_AD[1]	E
F				VDD	VDD	VDD	VSS	VSS	SPARE#	A_CLK OUT	VSS	ROM_SCK	A_AD[3]	F
G								VSS	DIV#	TEST#	SCAN_EN #	A_AD[7]	A_AD[4]	G
H								VDD	TRISTATE#	VDD_SYS	A_AD[8]	ADSTB[0]#	A_AD[6]	H
J								VDD	VDD_AGP	A_AD[0]	VSS	A_AD[9]	A_AD[10]	J
K								VDD	A_AD[2]	A_AD[5]	A_AD[14]	A_AD[11]	A_AD[12]	K
L	VSS	VSS	VSS						A_C/BE [0]#	A_AD[13]	A_PAR	A_SERR#	A_C/BE[1]#	L
M	VSS	VSS	VSS						A_AD[15]	A_STOP#	VSS	A_TRDY#	A_DEVSEL#	M
N	VSS	VSS	VSS						A_FRAME#	A_AD[16]	A_C/BE [2]#	A_VREF	A_IRDY#	N
P	VSS	VSS	VSS						A_AD[18]	A_AD[20]	A_AD[21]	A_AD[19]	A_AD[17]	P
R	VSS	VSS	VSS						A_AD[22]	A_C/BE [3]#	VSS	ADSTB[1]#	A_AD[23]	R
T	VSS	VSS	VSS						A_AD[26]	A_AD[24]	A_AD[29]	A_AD[27]	A_AD[25]	T
U								VDD	A_AD[30]	A_AD[28]	SBA[5]	SBA[6]	A_AD[31]	U
V								VDD	SBA[3]	SBA[7]	VSS	SBSTB#	SBA[4]	V
W								VDD	AD[0]	PIPE#	SBA[1]	SBA[0]	SBA[2]	W
Y								VSS	C/BE[0]#	AD[6]	ST[0]	ST[2]	RBF#	Y
AA				VDD	VDD	VDD	VSS	VSS	PAR	AD[11]	VSS	A_REQ#	ST[1]	AA
AB	CONNECT	GNT[2]#	AD[27]	GNT[3]#	AD[26]	AD[22]	AD[18]	FRAME#	STOP#	AD[13]	AD[2]	AD[1]	A_GNT#	AB
AC	CLK FWDRST	VTERM[2]	REQ[2]#	PGNT#	AD[28]	AD[24]	AD[20]	AD[16]	TRDY#	AD[15]	AD[5]	AD[4]	AD[3]	AC
AD	SADDIN [13]#	GNT[4]#	GNT[1]#	REQ[1]#	VSS	AD[31]	C/BE[3]#	VSS	C/BE[2]#	LOCK#	VSS	AD[8]	AD[7]	AD
AE	SADDIN CLK#	VSS	REQ[4]#	REQ[3]#	WSC#	AD[30]	AD[25]	AD[21]	AD[17]	DEVSEL#	C/BE[1]#	AD[12]	AD[9]	AE
AF	SADDIN [14]#	SADDIN [12]#	PROCRDY	GNT[0]#	REQ[0]#	PREQ#	AD[29]	AD[23]	AD[19]	IRDY#	SERR#	AD[14]	AD[10]	AF
	14	15	16	17	18	19	20	21	22	23	24	25	26	

AMD-751™ System Controller Functional Grouping—1 of 2

DRAM		DRAM		Processor		Processor		PCI	
Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
CS[0]#	C-14	MDAT[18]	B-18	CLKFWDRST	AC-14	SDATA[25]#	AC-7	AD[0]	W-22
CS[1]#	C-7	MDAT[19]	A-19	CONNECT	AB-14	SDATA[26]#	AD-6	AD[1]	AB-25
CS[2]#	D-7	MDAT[20]	C-19	PROCRDY	AF-16	SDATA[27]#	AB-7	AD[2]	AB-24
CS[3]#	D-6	MDAT[21]	B-20	RESET#	E-25	SDATA[28]#	AB-6	AD[3]	AC-26
CS[4]#	C-13	MDAT[22]	C-20	SADDIN[2]#	AF-11	SDATA[29]#	AC-5	AD[4]	AC-25
CS[5]#	A-13	MDAT[23]	B-21	SADDIN[3]#	AF-12	SDATA[30]#	AA-5	AD[5]	AC-24
DQM[0]#	A-5	MDAT[24]	A-22	SADDIN[4]#	AD-13	SDATA[31]#	AB-4	AD[6]	Y-23
DQM[1]#	A-6	MDAT[25]	B-22	SADDIN[5]#	AD-11	SDATA[32]#	Y-5	AD[7]	AD-26
DQM[2]#	A-15	MDAT[26]	A-23	SADDIN[6]#	AD-12	SDATA[33]#	Y-4	AD[8]	AD-25
DQM[3]#	B-15	MDAT[27]	B-23	SADDIN[7]#	AB-12	SDATA[34]#	W-5	AD[9]	AE-26
DQM[4]#	B-5	MDAT[28]	A-24	SADDIN[8]#	AB-13	SDATA[35]#	V-5	AD[10]	AF-26
DQM[5]#	B-6	MDAT[29]	A-25	SADDIN[9]#	AF-13	SDATA[36]#	U-4	AD[11]	AA-23
DQM[6]#	E-16	MDAT[30]	E-23	SADDIN[10]#	AE-13	SDATA[37]#	V-3	AD[12]	AE-25
DQM[7]#	D-17	MDAT[31]	A-26	SADDIN[11]#	AE-11	SDATA[38]#	W-3	AD[13]	AB-23
MAdA[0]	B-8	MDAT[32]	L-4	SADDIN[12]#	AF-15	SDATA[39]#	V-1	AD[14]	AF-25
MAdA[1]	C-8	MDAT[33]	K-4	SADDIN[13]#	AD-14	SDATA[40]#	AC-1	AD[15]	AC-23
MAdA[2]	B-9	MDAT[34]	G-1	SADDIN[14]#	AF-14	SDATA[41]#	AB-3	AD[16]	AC-21
MAdA[3]	A-8	MDAT[35]	K-5	SADDINCLK#	AE-14	SDATA[42]#	AB-2	AD[17]	AE-22
MAdA[4]	C-10	MDAT[36]	J-4	SADDOUT[2]#	M-1	SDATA[43]#	AB-1	AD[18]	AB-20
MAdA[5]	A-9	MDAT[37]	F-2	SADDOUT[3]#	N-1	SDATA[44]#	Y-2	AD[19]	AF-22
MAdA[6]	A-10	MDAT[38]	H-4	SADDOUT[4]#	N-4	SDATA[45]#	Y-1	AD[20]	AC-20
MAdA[7]	B-10	MDAT[39]	E-2	SADDOUT[5]#	L-2	SDATA[46]#	U-5	AD[21]	AE-21
MAdA[8]	B-11	MDAT[40]	G-4	SADDOUT[6]#	L-3	SDATA[47]#	W-2	AD[22]	AB-19
MAdA[9]	C-11	MDAT[41]	G-5	SADDOUT[7]#	J-3	SDATA[48]#	T-5	AD[23]	AF-21
MAdA[10]	A-11	MDAT[42]	D-2	SADDOUT[8]#	L-1	SDATA[49]#	P-2	AD[24]	AC-19
MAdA[11]	A-12	MDAT[43]	F-5	SADDOUT[9]#	K-3	SDATA[50]#	R-5	AD[25]	AE-20
MAdA[12]	E-17	MDAT[44]	C-1	SADDOUT[10]#	M-3	SDATA[51]#	T-4	AD[26]	AB-18
MAdA[13]	B-12	MDAT[45]	E-4	SADDOUT[11]#	M-5	SDATA[52]#	P-5	AD[27]	AB-16
MAdA[14]	B-13	MDAT[46]	E-5	SADDOUT[12]#	K-2	SDATA[53]#	P-1	AD[28]	AC-18
MAdB[0]	E-9	MDAT[47]	A-1	SADDOUT[13]#	J-1	SDATA[54]#	P-4	AD[29]	AF-20
MAdB[1]	D-9	MDAT[48]	E-18	SADDOUT[14]#	H-1	SDATA[55]#	N-5	AD[30]	AE-19
MAdB[2]	E-10	MDAT[49]	A-18	SADDOUTCLK#	K-1	SDATA[56]#	W-1	AD[31]	AD-19
MAdB[3]	D-10	MDAT[50]	D-19	SCHECK[0]#	AD-7	SDATA[57]#	U-3	C/BE[0]#	Y-22
MAdB[4]	E-11	MDAT[51]	B-19	SCHECK[1]#	AB-10	SDATA[58]#	U-2	C/BE[1]#	AE-24
MAdB[5]	D-11	MDAT[52]	A-20	SCHECK[2]#	AE-3	SDATA[59]#	U-1	C/BE[2]#	AD-22
MAdB[6]	D-12	MDAT[53]	E-19	SCHECK[3]#	AC-4	SDATA[60]#	T-2	C/BE[3]#	AD-20
MAdB[7]	E-13	MDAT[54]	A-21	SCHECK[4]#	W-4	SDATA[61]#	R-3	DEVSEL#	AE-23
MAdB[8]	D-13	MDAT[55]	D-20	SCHECK[5]#	AA-1	SDATA[62]#	T-1	FRAME#	AB-21
MAdB[9]	E-12	MDAT[56]	E-20	SCHECK[6]#	N-3	SDATA[63]#	P-3	GNT[0]#	AF-17
MAdB[10]	E-14	MDAT[57]	C-22	SCHECK[7]#	T-3	SDATAINCLK[0]#	AD-8	GNT[1]#	AD-16
MAdB[11]	E-15	MDAT[58]	D-21	SDATA[0]#	AF-8	SDATAINCLK[1]#	AB-5	GNT[2]#	AB-15
MAdB[12]	A-16	MDAT[59]	C-23	SDATA[1]#	AB-9	SDATAINCLK[2]#	Y-3	GNT[3]#	AB-17
MAdB[13]	D-14	MDAT[60]	B-24	SDATA[2]#	AF-7	SDATAINCLK[3]#	R-1	GNT[4]#	AD-15
MAdB[14]	D-15	MDAT[61]	E-21	SDATA[3]#	AE-8	SDATAINVAL#	AC-13	IRDY#	AF-23
MCKE[0]	D-16	MDAT[62]	D-22	SDATA[4]#	AE-7	SDATAOUTCLK[0]#	AC-11	LOCK#	AD-23
MCKE[1]	B-14	MDAT[63]	E-22	SDATA[5]#	AF-6	SDATAOUTCLK[1]#	AC-2	PAR	AA-22
MCKE[2]	A-14	MECCD[0]	B-2	SDATA[6]#	AF-5	SDATAOUTCLK[2]#	AA-3	PCLK	D-25
MDAT[0]	L-5	MECCD[1]	B-3	SDATA[7]#	AF-4	SDATAOUTCLK[3]#	N-2	PGNT#	AC-17
MDAT[1]	H-2	MECCD[2]	B-16	SDATA[8]#	AC-10	SYSCLK	B-26	PREQ#	AF-19
MDAT[2]	H-3	MECCD[3]	A-17	SDATA[9]#	AF-10	VREF	AF-1	WSC#	AE-18
MDAT[3]	G-2	MECCD[4]	A-2	SDATA[10]#	AB-11			REQ[0]#	AF-18
MDAT[4]	G-3	MECCD[5]	A-3	SDATA[11]#	AE-10			REQ[1]#	AD-17
MDAT[5]	F-1	MECCD[6]	C-16	SDATA[12]#	AD-9			REQ[2]#	AC-16
MDAT[6]	E-1	MECCD[7]	D-18	SDATA[13]#	AF-9			REQ[3]#	AE-17
MDAT[7]	J-5	SCAS[0]#	A-4	SDATA[14]#	AD-10			REQ[4]#	AE-16
MDAT[8]	H-5	SCAS[1]#	D-5	SDATA[15]#	AC-8			SERR#	AF-24
MDAT[9]	E-3	SCAS[2]#	C-4	SDATA[16]#	AE-5			STOP#	AB-22
MDAT[10]	D-1	SRAS[0]#	B-7	SDATA[17]#	AD-5			TRDY#	AC-22
MDAT[11]	D-3	SRAS[1]#	D-8	SDATA[18]#	AE-4				
MDAT[12]	F-4	SRAS[2]#	A-7	SDATA[19]#	AD-3				
MDAT[13]	C-2	WE[0]#	C-5	SDATA[20]#	AF-2				
MDAT[14]	B-1	WE[1]#	E-6	SDATA[21]#	AE-2				
MDAT[15]	D-4	WE[2]#	B-4	SDATA[22]#	AE-1				
MDAT[16]	B-17	CLKIN	E-8	SDATA[23]#	AD-2				
MDAT[17]	C-17	CLKOUT	E-7	SDATA[24]#	AB-8				

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AGP		AGP/PCI		VSS	VSS	VDD	MISC	
Pin Name	Pin No.	Pin Name	Pin No.	Pin No.	Pin No.	Pin No.	Pin Name	Pin No.
ADSTB[0]#	H-25	A_AD[0]	J-23	AD-1	L-14	H-6	A_CLKOUT	F-23
ADSTB[1]#	R-25	A_AD[1]	E-26	J-2	M-14	J-6	BYPASS#	C-25
PIPE#	W-23	A_AD[2]	K-22	M-2	N-14	K-6	DCSTOP#	E-24
RBF#	Y-26	A_AD[3]	F-26	R-2	P-14	F-8	DIV#	G-22
SBA[0]	W-25	A_AD[4]	G-26	V-2	R-14	F-9	REF_5V	D-23
SBA[1]	W-24	A_AD[5]	K-23	AA-2	T-14	F-10	ROM_SCK	F-25
SBA[2]	W-26	A_AD[6]	H-26	C-3	C-15	F-17	ROM_SDA	D-26
SBA[3]	V-22	A_AD[7]	G-25	F-3	L-15	AA-17	S_CLKOUT	D-24
SBA[4]	V-26	A_AD[8]	H-24	AC-3	M-15	F-18	S_CLKREF	C-26
SBA[5]	U-24	A_AD[9]	J-25	AF-3	N-15	AA18	SCAN_EN#	G-24
SBA[6]	U-25	A_AD[10]	J-26	C-6	P-15	F-19	SPARE#	F-22
SBA[7]	V-23	A_AD[11]	K-25	F-6	R-15	AA-19	TEST#	G-23
SBSTB#	V-25	A_AD[12]	K-26	G-6	T-15	H-21	TRISTATE#	H-22
ST[0]	Y-24	A_AD[13]	L-23	U-6	AE-15	J-21	VDD_SYS	H-23
ST[1]	AA-26	A_AD[14]	K-24	V-6	L-16	K-21	VTERM[0]	AA-4
ST[2]	Y-25	A_AD[15]	M-22	W-6	M-16	U-21	VTERM[1]	AC-12
VDD_AGP	J-22	A_AD[16]	N-23	Y-6	N-16	V-21	VTERM[2]	AC-15
		A_AD[17]	P-26	AA-6	P-16	W-21	VTERM[3]	AC-6
		A_AD[18]	P-22	AE-6	R-16		VTERM[4]	AC-9
		A_AD[19]	P-25	F-7	T-16		VTERM[5]	AD-4
		A_AD[20]	P-23	AA-7	C-18		VTERM[6]	M-4
		A_AD[21]	P-24	AA-8	AD-18		VTERM[7]	R-4
		A_AD[22]	R-22	C-9	F-20		VTERM[8]	V-4
		A_AD[23]	R-26	AA-9	AA-20			
		A_AD[24]	T-23	AE-9	C-21			
		A_AD[25]	T-26	AA-10	F-21			
		A_AD[26]	T-22	L-11	G-21			
		A_AD[27]	T-25	M-11	Y-21			
		A_AD[28]	U-23	N-11	AA-21			
		A_AD[29]	T-24	P-11	AD-21			
		A_AD[30]	U-22	R-11	C-24			
		A_AD[31]	U-26	T-11	F-24			
		A_C/BE[0]#	L-22	C-12	J-24			
		A_C/BE[1]#	L-26	L-12	M-24			
		A_C/BE[2]#	N-24	M-12	R-24			
		A_C/BE[3]#	R-23	N-12	V-24			
		A_CLK	B-25	P-12	AA-24			
		A_DEVSEL#	M-26	R-12	AD-24			
		A_FRAME#	N-22	T-12				
		A_GNT#	AB-26	AE-12				
		A_IRDY#	N-26	L-13				
		A_PAR	L-24	M-13				
		A_REQ#	AA-25	N-13				
		A_SERR#	L-25	P-13				
		A_STOP#	M-23	R-13				
		A_TRDY#	M-25	T-13				
		A_VREF	N-25					

12 Package Specifications

Figure 35 and Figure 36 on page 202 show the package specifications for the AMD-751 system controller. Tables 39, 40, and 41, starting on page 203, contain information about the symbols shown in the figures.

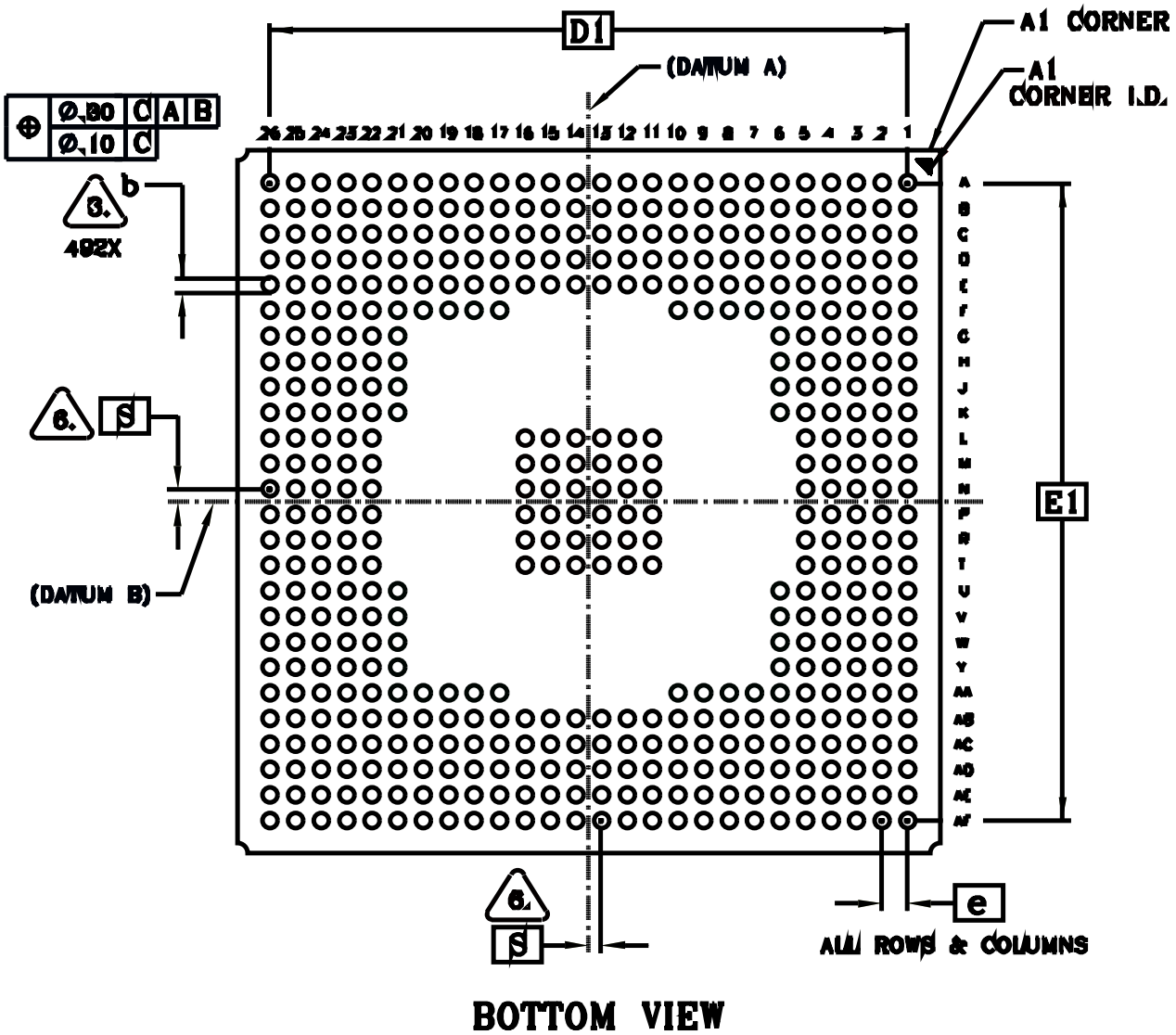

Figure 35. Bottom Side View of Package

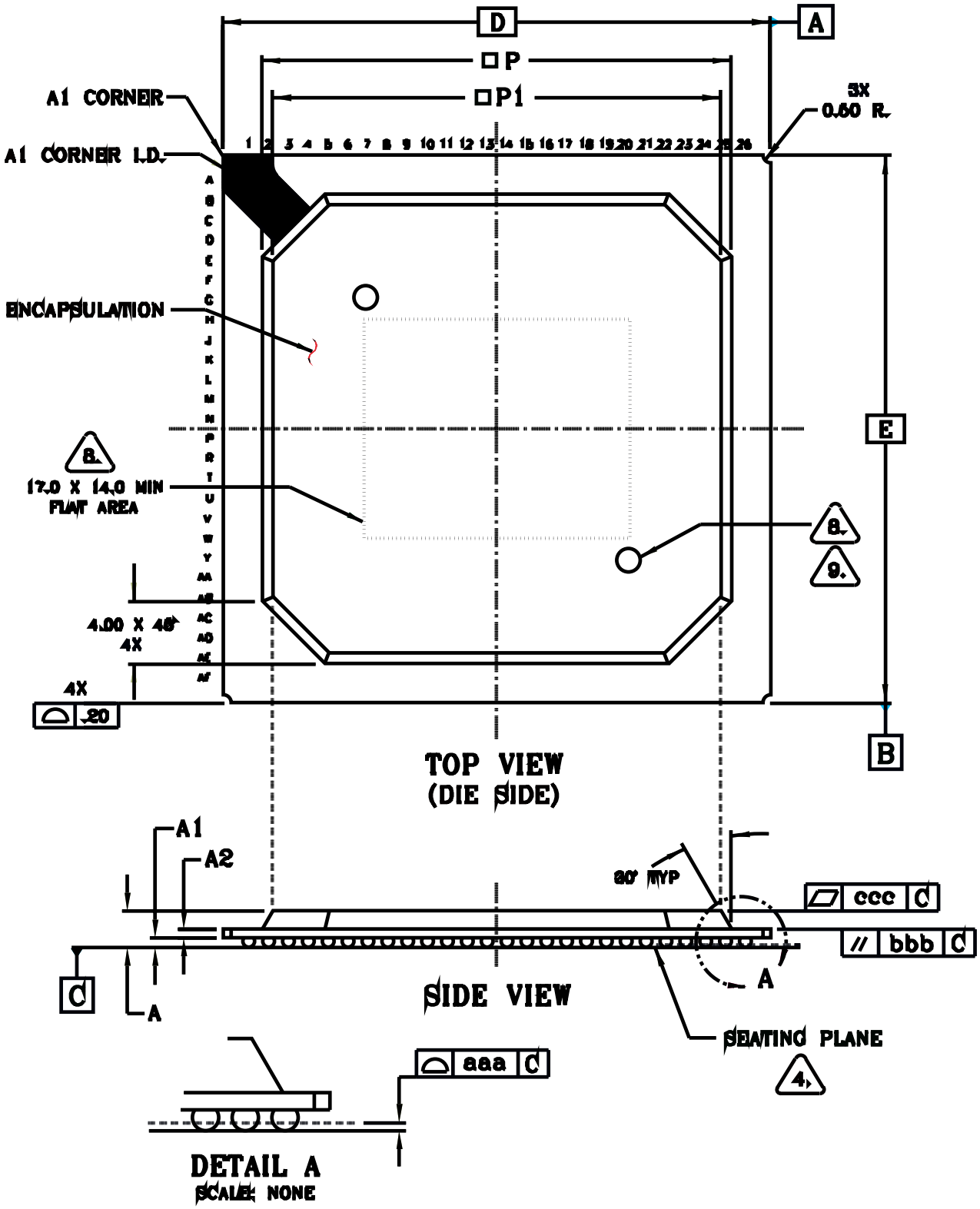

Figure 36. Top and Side Views of Package

Table 39. Symbol Notes

Symbol	Description
1	Dimensions and tolerances conform to ASME Y14.5M–1994.
2	All dimensions are in millimeters.
3	Dimension 'b' is measured at the maximum solder ball diameter on a plane parallel to Datum C.
4	Datum C and the seating plane are defined by the spherical crowns of the solder balls.
5	The number of peripheral rows and columns.
6	'S' is measured with respect to Datums A and B, and defines the position of the solder balls nearest the package centerlines.
7	Conforms to JEP-95, MO-151, Issue 9, Variation Bal-2.
8	The minimum flat area top side of the package is used for marking and pickup. The flatness specification applied to this area. Any ejector marks must be outside of this area.
9	Optional features.

Table 40. 492-Pin PBGA 35.0 mm By 35.0 mm Package Specifications

Symbol	Minimum	Nominal	Maximum	Description
A	2.20	2.33	2.46	Overall thickness
A1	0.50	0.60	0.70	Ball height
A2	0.51	0.56	0.61	Body thickness
D	35.00 BSC.			Body size
D1	31.75 BSC.			Ball footprint
E	35.00 BSC.			Body size
E1	31.75 BSC.			Ball footprint
M	26 x 26			Ball matrix size
N	492			Total ball count
MR	5			Number of rows 5
b	0.60	0.75	0.90	Ball diameter
e	1.27 BSC.			Ball pitch
P	29.9	30.0	30.1	Encapsulation area
P1	28.0 Minimum			Flat encapsulation area
S	0.635 BSC.			Solder ball placement

Table 41. Geometric Tolerances

Symbol	Tolerance	Description
aaa	0.15	Coplanarity
bbb	0.15	Parallelism
ccc	0.15	Flatness

Index

Numerics

A

B

C

D

E

F

G

H

I

J

L

M

N

O

P

R

S

T

U

V

W

X

Z